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LIGHTWEIGHT MULTIPLE OUTPUT CONVERTER DEVELOPMENT

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OUTPUT CONVERTER DEVELOPMENT (Hughes
Aircraft Co.) 75 p HC A04/MF A01 CSCL 09C

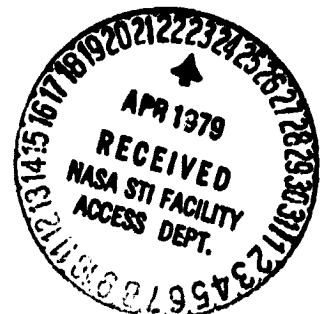
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PREPARED FOR
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
NASA LEWIS RESEARCH CENTER
CONTRACT NAS 3-21045



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FOREWORD

This report documents work performed by the Hughes Aircraft Company during the period of 1 October 1977 to 1 November 1978 for the NASA Lewis Research Center under Contract NAS 3-21045. The NASA Project Manager was William T. Harrigill. The Program Manager at Hughes Aircraft Company was Jack J. Kisch. Mr. Robert M. Martinelli was responsible for the circuit design.

ABSTRACT

A high frequency, multiple output power conditioner was developed and breadboarded using an eight-stage capacitor diode voltage multiplier to provide +1200 Vdc, and a three-stage for -350 Vdc. In addition, two rectifier bridges were capacitively coupled to the eight-stage multiplier to obtain 0.5 a dc and 0.65 a dc constant current outputs referenced to +1200 Vdc. Total power was 120 watts, with an overall efficiency of 85 percent at the 80 kHz operating frequency. All outputs were regulated to three percent or better, with complete short circuit protection.

The power conditioner component weight and efficiency was compared to the equivalent four outputs of the 10 kHz conditioner for the 8 cm ion engine. Weight reduction for the four outputs was 557 grams; extrapolated in the same ratio to all nine outputs, it would be 1100 to 1400 grams.

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1.0 INTRODUCTION

Capacitor-diode voltage multiplier (CDVM) power supplies have been used for many years, commencing with an 800 kV supply for an ion accelerator built by Cockroft and Walton in 1932.¹ Because of technology limitations, CDVM circuits have been used primarily for high voltage, low current applications. The use of CDVM circuits reduce the size of the high voltage transformer and, in some cases, makes it possible to eliminate the transformer entirely, resulting in a significant size and weight savings over conventional step-up transformer-rectifier-filter circuits. These advantages would be of prime interest for space applications involving equipment requiring high voltages at low currents.

Only recently, because of new technological developments, has the CDVM circuit been considered for high efficiency, low weight power supplies delivering a considerable amount of power. These developments have made it possible to design CDVM converters with an efficiency comparable to that of the more conventional transformer-rectifier-filter circuit, but with a significant weight saving. Major developments in the component field have contributed to this possibility, two of which are: (1) the recent availability of much faster switching diodes and transistors, allowing the converter to operate at higher frequencies, reducing proportionally the total capacitance required in the CDVM, and (2) the development of high power density capacitors using dielectrics of polyvinylidene fluoride (PVF2) or polysulfone films has resulted in a significant reduction in the size and weight of the CDVM capacitors themselves. Based on the work of W. T. Harrigill and I. T. Meyers^{2, 3, 4} of the NASA Lewis Research Center on CDVM converters operating at 50 to 200 kHz, Hughes Aircraft, on a previous program, developed a 1200 Vdc, 100 W regulated output CDVM converter using the newly

developed components noted above. Tests showed an efficiency in excess of 90 percent with a component weight of 197 grams.⁵

Up to now, the development of CDVM power supplies has been concerned only with a single voltage output; however, many applications require several voltages. Rather than have a separate supply for each voltage, the objective of this program was to develop the technology for multiple output supplies which derive their voltages from taps in the CDVM network. Also, at times it is desired to reference these voltage outputs to potentials other than ground. An additional objective was to demonstrate the weight savings of operating the converters at frequencies in excess of 50 kilohertz to project the potential advantages of a high frequency, multiple output CDVM based design for applications such as the 8 cm ion engine.

A breadboard model of a multiple output CDVM power supply was designed, fabricated, and tested, having two regulated output voltages referenced to ground and two regulated output currents referenced to the output voltages. Weight was under 200 grams with an operating frequency of 80 kHz. Information derived from this model demonstrated that the use of the high frequency technology could result in appreciable weight savings. For example, a power supply based on the above results for the 8 cm ion engine could result in a weight saving of 25 to 50 percent, while only reducing the efficiency by 1 to 2 percent as compared to the existing 10 kHz design.

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2.0 CIRCUIT DESIGN CONSTRAINTS

Two power supply designs are called out in the Statement of Work, Appendix B. The Type I circuit is a single low-voltage, high current supply biased at a high voltage by a CDVM supply, while the Type II consists of three power supplies operating simultaneously from the input of a CDVM.

2.1 TYPE I CDVM BIASED POWER SUPPLY DESIGN

A low voltage, high current regulated power supply biased at a high voltage by a capacitor diode voltage multiplier as shown in Figure 2-1 was designed to meet the constraints shown in Table 2-1. The design was based on other NASA CDVM work, and present state-of-the-art. Short circuit protection was required for both supplies. Pulse-width modulation was used in a buck-boost circuit to achieve the desired regulation.

Performance of the Type I power supply was evaluated by building and testing a breadboard circuit, which essentially met the requirements of Table 2-1. A magnetic amplifier regulator circuit was substituted for the buck-boost regulator circuit for comparison of weight and performance trade-offs. It was found that the mag-amp approach made the attainment of short circuit protection much easier, at less weight and higher efficiency; however, because of the desires to minimize magnetic components, and investigate new approaches, the decision was made to use the buck, or buck-boost circuits to meet the regulation requirements. The breadboard for the Type I circuit is specified as a nondeliverable engineering breadboard.

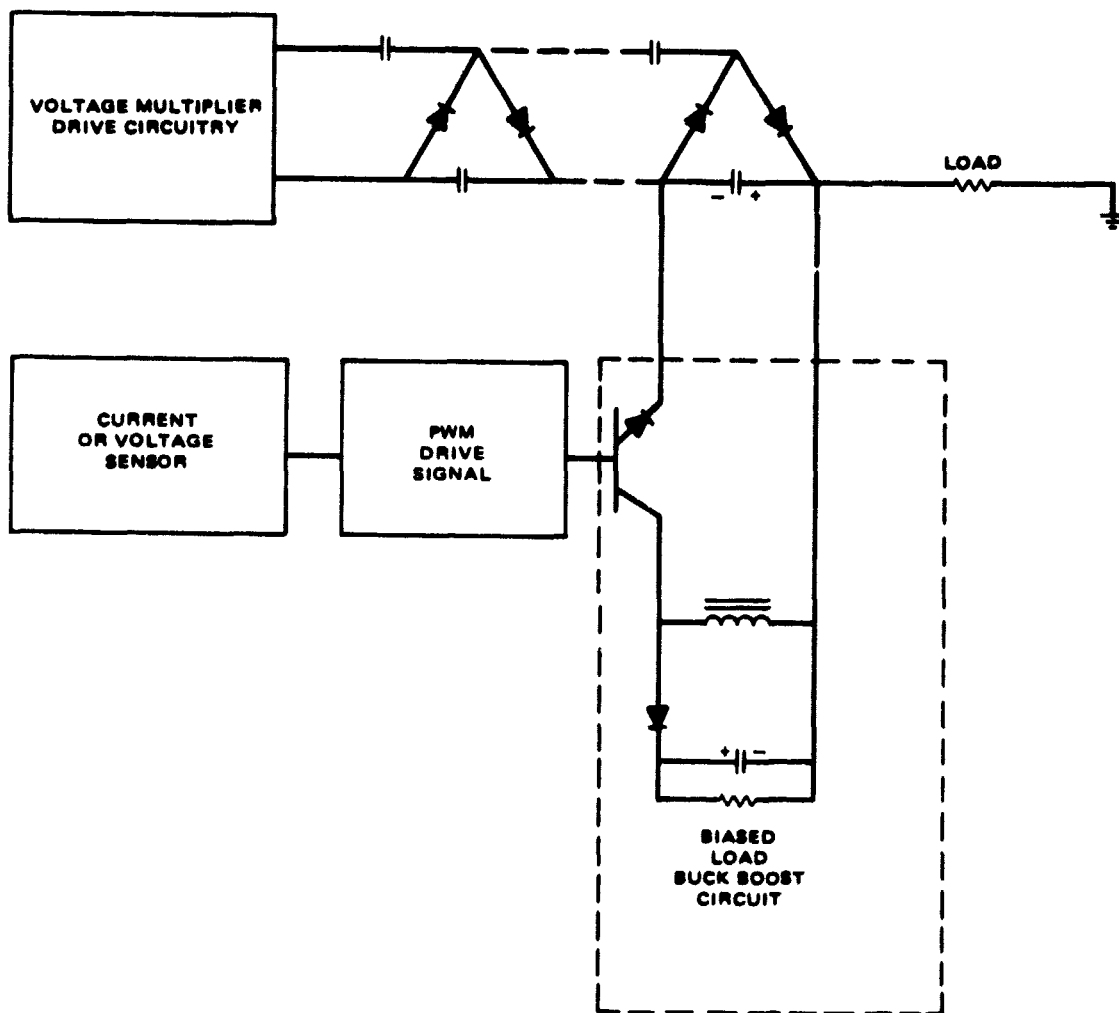


Figure 2-1. Biased supply driven by CDVM.

TABLE 2-1. TYPE I POWER SUPPLY REQUIREMENTS

Input Voltage	110 - 130 Vdc	
CDVM Output	1200 Vdc	16.7 - 67.0 MA
Output Voltage Regulation	±1%	
Output Voltage Ripple	<1% pp	
Frequency	>50 kHz	
Efficiency at Max Load	>90%	
Biased Supply No. 1 Output	38 - 42 Vdc	100 - 650 MA
Output Current Regulation	±3%	
Output Current Ripple	<1% pp	
Frequency	>50 kHz	
Efficiency at Max Load	>80%	
Overall Efficiency at Max Load	88%	

2.2 TYPE II MULTIPLE BIASED POWER SUPPLIES

Based on the test results of the Type I power supply above, and the previous NASA report⁵, multiple biased supplies driven by a CDVM are shown in the block diagram of Figure 2-2. Table 2-2 below summarizes the four output requirements.

Design of the +1200 Vdc and the -350 Vdc supplies were based on the high frequency CDVM technology previously developed by Hughes under NASA contract NAS 3-20111.⁵ The two current regulated supplies were to be pulse width modulated current regulators fed from voltage taps on the last stage of the CDVM. The converter was short circuit protected for a single fault or any combination of shorts across any supply output and its return or faults connecting any two outputs together. The design goal for the efficiency of the converter was to exceed 86 percent.

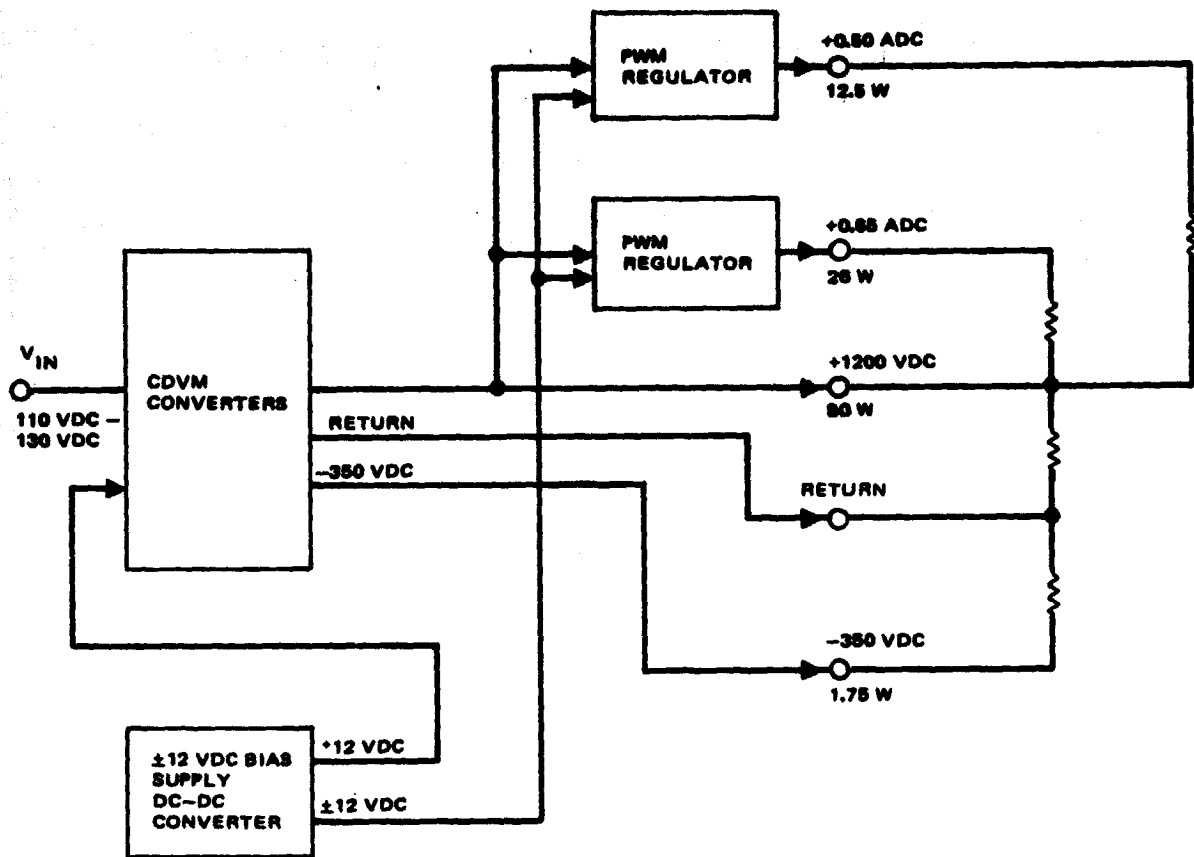


Figure 2-2. Block diagram, multiple output CDVM converter.

TABLE 2-2. TYPE II POWER SUPPLY REQUIREMENTS

Output	Regulation	Power	Referenced to
+1200 Vdc	±1%	80 W	GND
-350 Vdc	±3%	1.75 W	GND
+0.65 Adc	±3%	26 W	1200 Vdc
+0.50 Adc	±3%	12.5 W	-350 Vdc

2.3 CAPACITOR-DIODE VOLTAGE MULTIPLIER

2.3.1 Two-Phase Versus Single Phase CDVM

Two-phase capacitor diode voltage multiplier circuits were selected for the +1200 Vdc and the -350 Vdc outputs. Simplified schematics for the two supplies are shown in Figures 2-3(b) and 2-4 respectively. The two-phase

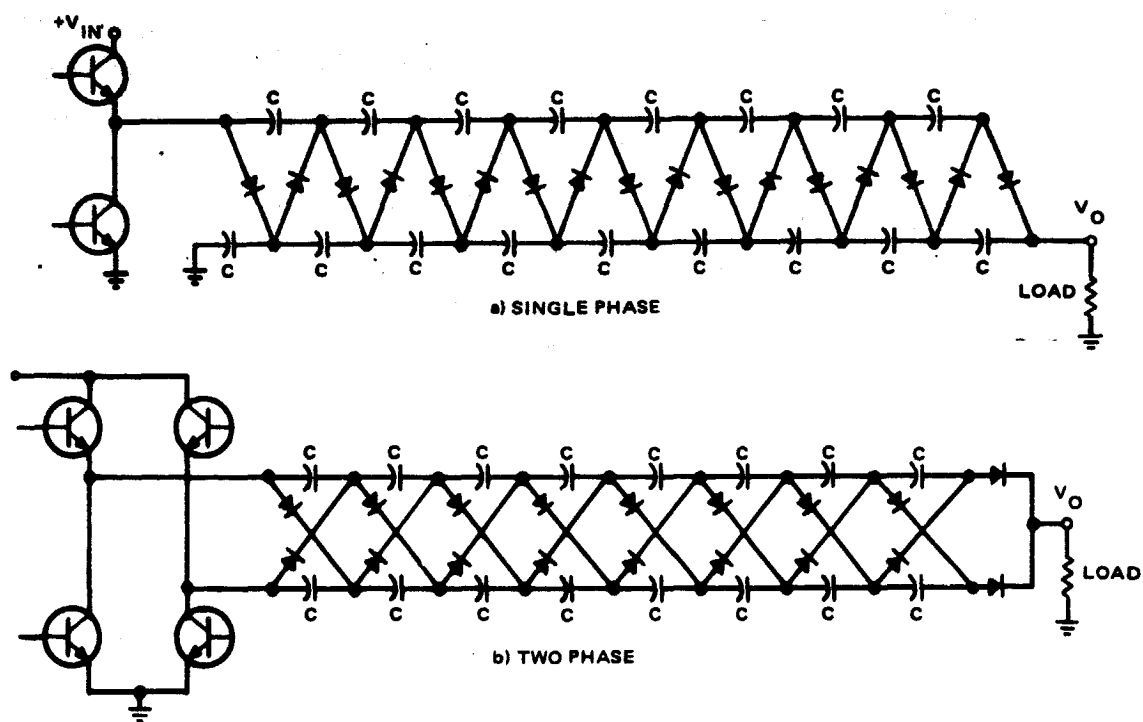


Figure 2-3. Comparison of single phase and two-phase capacitor diode voltage multiplier circuits.

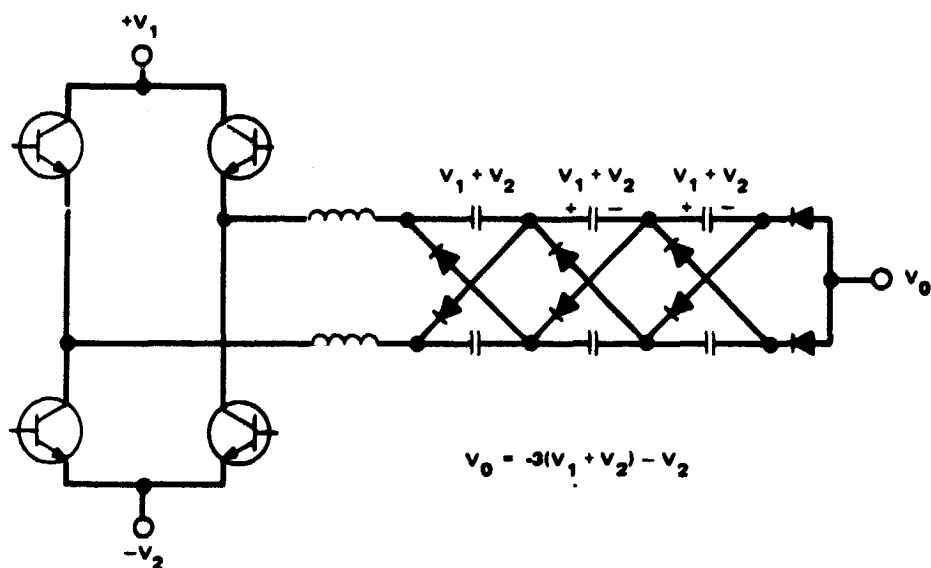


Figure 2-4. Negative output CDVM.

circuit was selected over the single phase because it was previously demonstrated under contract NAS 3-20111 that the two-phase circuit has some inherent advantages. Figure 2-3 shows simplified schematics comparing the 1200 Vdc single phase and two phase configurations. The multiplier parts count is identical for both, but the two phase requires an additional set of drive transistors and components. It is felt that the lower total capacitance, improved efficiency due to lower rectifier losses and reduced output ripple voltage and input ripple current (lower EMI) of the two-phase circuit more than offsets the increase in drive components.

2.3.2 Description of Operation of Two-Phase CDVM

In general, a capacitor diode voltage multiplier circuit (CDVM) consists of pairs of capacitors and diodes connected in sequence, which steps up and converts an ac voltage to a dc output voltage. This output voltage is a fixed multiple of the peak-to-peak input voltage, depending on the number of capacitor-diode sets.

Figure 2-3(a) demonstrates a single phase CDVM using 9 capacitor-diode sets driven by a transistor chopper as an ac input source. The output voltage of this circuit, assuming ideal rectifiers and ideal transistor switches, is 9 times the input voltage. Figure 2-3(b) shows a two-phase CDVM circuit with an identical dc voltage output which was developed at Hughes Aircraft.

Figure 2-5 demonstrates the operation of a two-phase CDVM circuit. When the input to phase A is high, capacitor C18 in Figure 2-5(a) is connected to the load through the output rectifier. The average current through the rectifier (and capacitor) over a half cycle is equal to the load current. In that same half cycle, the average current in C17 will be 2 times the load current since it will carry the same current that flows through C18 in addition to the current that flows through CR8. The average currents through the capacitors become progressively larger near the input terminal. In the steady state condition, when phase A goes to zero and phase B goes high, Figure 2-5(b), the average currents through the capacitors must be of the same magnitude but in the opposite direction from the previous half cycle.

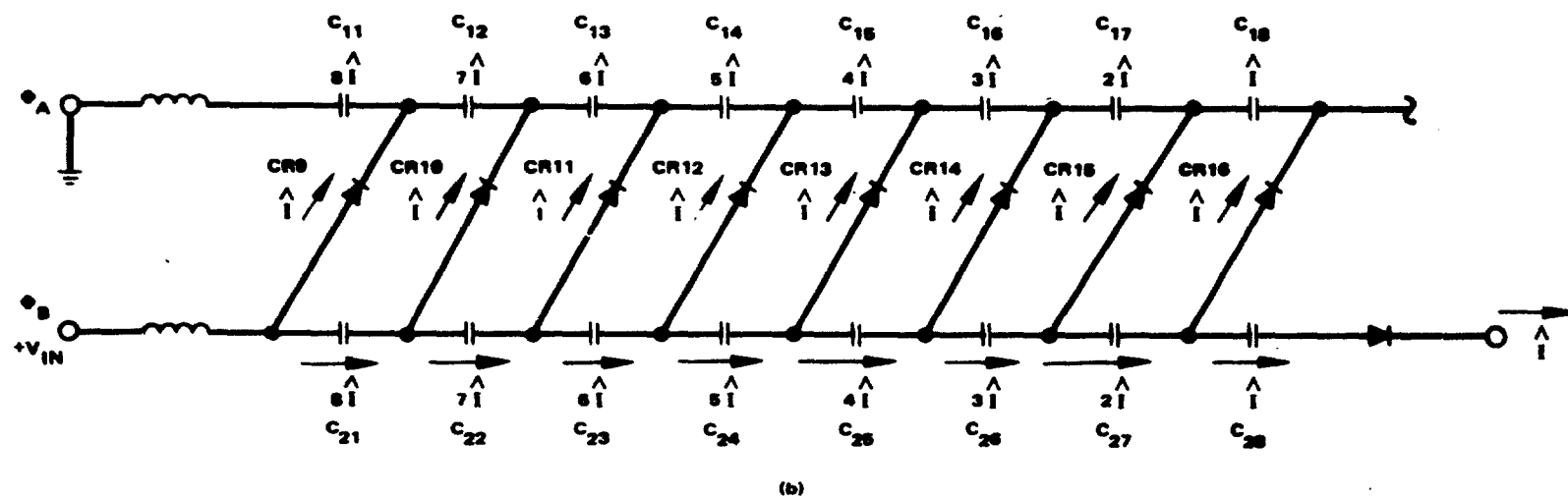
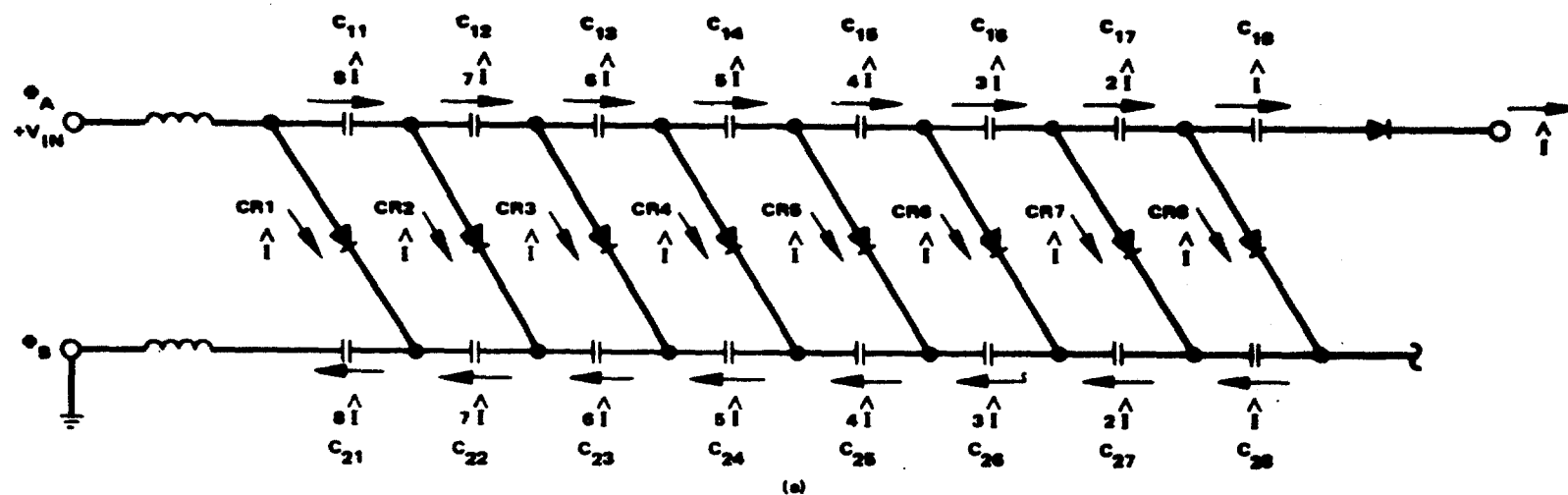


Figure 2-5. Current paths in a two-phase CDVM.

Input inductors are employed in series with each phase of the CDVM to improve the efficiency of the circuit. In general, the inductor values are selected to resonate with the CDVM capacitance at the switching frequency so that the peak current will be minimized and the current will be nearly zero when the transistor switches. Figure 2-6 demonstrates typical CDVM input currents when the inductor values are properly chosen.

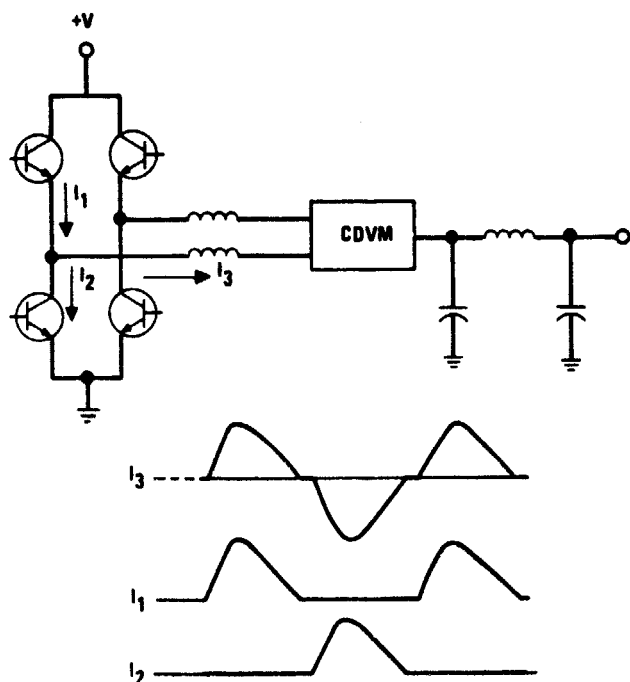


Figure 2-6. Typical transistor currents.

2.4 REGULATION

Under the previous contract NAS 3-20111 mentioned above, it was demonstrated that the output voltage of the CDVM could be regulated in a closed loop fashion. Given a dual input voltage to the transistor chopper of $+V_1$ and $-V_2$, the latter instead of ground as shown in Figure 2-7 in the ideal case where rectifier and transistor forward voltages are assumed to be zero, the average output from the CDVM will be approximately $8(V_1 + V_2) + V_1$. If the output voltage is sensed and used to control only the negative input voltage to the transistor chopper, the average output voltage from the CDVM can be controlled as accurately as the sensing circuitry allows.

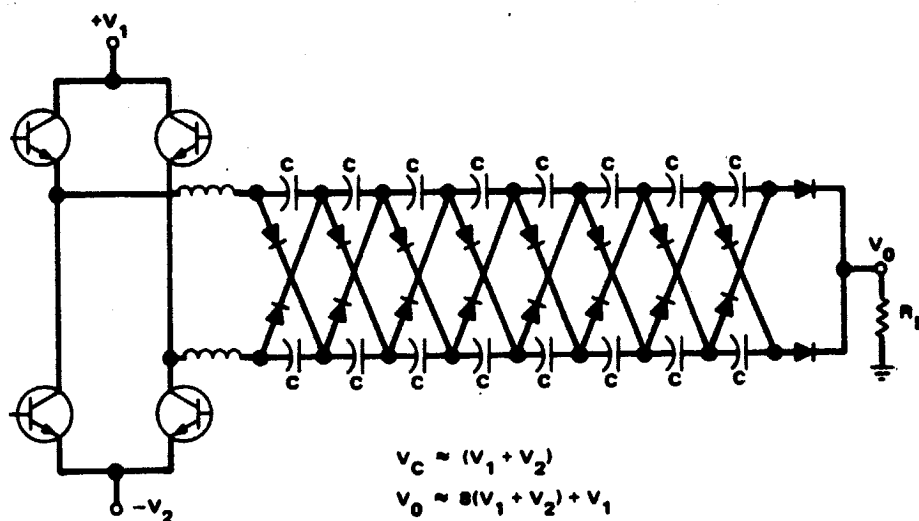


Figure 2-7. Two-phase CDVM regulation technique.

2.5 SHORT CIRCUIT CURRENT LIMITATION

To protect the components in the CDVM in the event of a short circuit on the output, some form current limiting must be applied. In this application it was previously decided to sense the output current and inhibit drive to the transistor bridge circuit if the output current exceeded some maximum limit. However, if a sudden short were applied to the output, the resulting peak currents due to the CDVM capacitors rapidly discharging might be sufficient to damage the diodes and capacitors, even if the transistor turned off immediately. An inductor in series with the CDVM output was used to limit the peak currents. With the proper value of inductance, the discharge of the CDVM stored energy can be controlled to acceptable limits.

Selecting the allowable peak current I_p , with the known capacitor voltage V_{in} , and the total capacitance C_{TOT} , the minimum inductance was calculated. The peak current in the inductor occurs when all of the stored energy in the CDVM has been transferred to the inductor. The total energy stored in the CDVM capacitors is

$$E_c = \frac{1}{2} C_{TOT} V_{in}^2$$

If the total energy in the CDVM is transferred to the inductor, the peak current will be limited by selecting the proper inductance value. Solving the energy equation for inductance gives the minimum allowed inductor value

$$E_L = \frac{1}{2} L I_p^2 = E_c$$

$$L_{\min} = \frac{E_c}{\frac{1}{2} I_p^2} = \frac{\frac{1}{2} C_{TOT} V_{in}^2}{\frac{1}{2} I_p^2}$$

$$L_{\min} = \frac{C_{TOT} V_{in}^2}{I_p^2}$$

to limit the peak currents in the CDVM to I_p .

2.6 VOLTAGES REFERENCED TO OTHER THAN GROUND

If a dc voltage referenced to the output of a CDVM is required, it is possible to provide a voltage tap in the following manner. Figure 2-8 shows two rectifier bridges, one directly connected to the ac source, the other connected through capacitors. The voltage V_1 is equal to the peak ac voltage. As long as capacitor impedances at the source frequency are significantly lower than the load resistance, the dc voltage V_2 across the load R_2 , will be equal to the peak ac voltage. Since the coupling capacitors block dc, V_2 can be referenced to V_1 by the connection shown as a dashed line.

This same principle may be applied to CDVM design. The ac voltage supplied through the CDVM is capacitively coupled to a bridge rectifier circuit as shown in Figure 2-9, where CR1 through CR4 are the bridge rectifiers while C1 and C2 are the ac coupling capacitors. As shown in the figure, there are two outputs, V_{01} , a high voltage output referenced to ground, and V_{02} , a low voltage output referenced to the high voltage output.

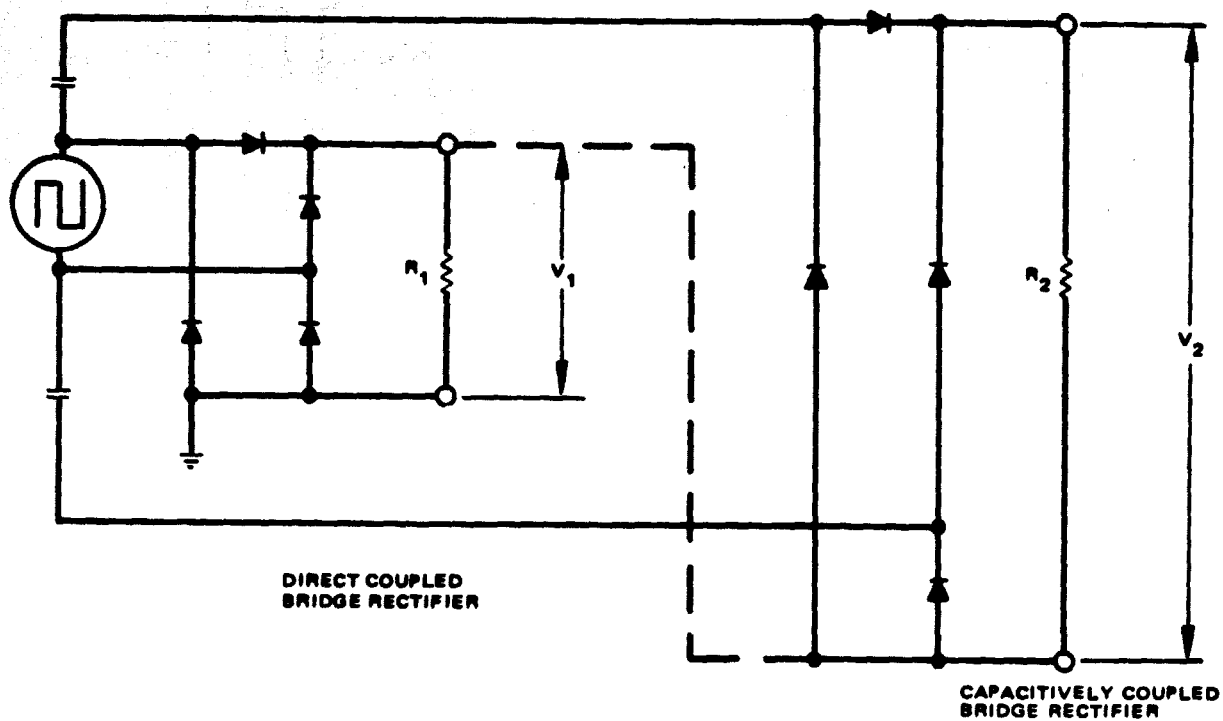
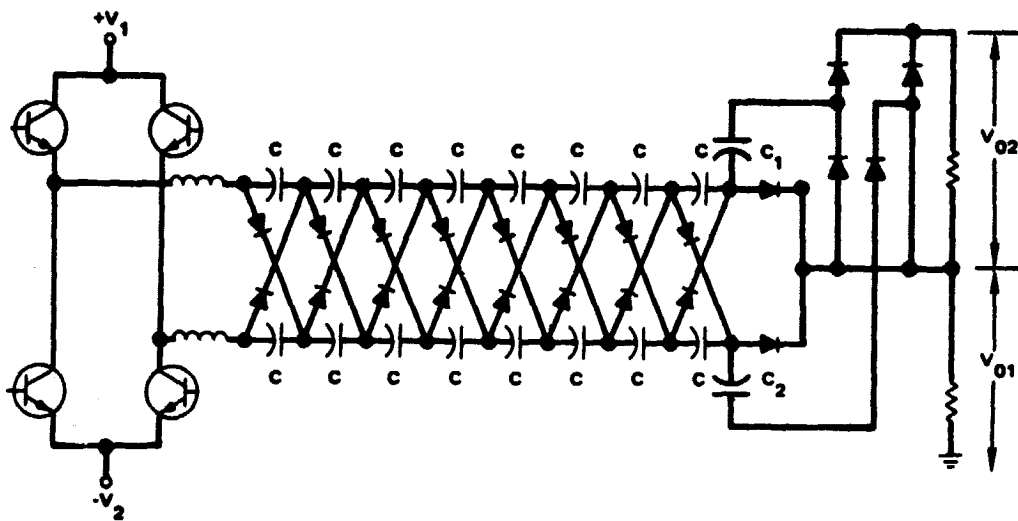


Figure 2-8. Direct and capacitively coupled bridge rectifiers driven by common circuit.



$$V_{01} \approx 8(V_1 + V_2) + V_1$$

$$V_{02} \approx V_1 + V_2$$

Figure 2-9. DC isolation of bridge rectifier connected to CDVM output.

2.7 CONSTANT CURRENT REGULATED SUPPLIES

According to the statement of work, the supplies referenced to 1200 Vdc are constant current, regulated pulse width modulated converters as shown in the block diagram of Figure 2-2. Two basic configurations were considered: a buck-boost regulator and a buck regulator. A design comparison between the two configurations was initiated to determine the circuit which would be employed in the converter design. Figures 2-10 and 2-11 demonstrate the basic circuit topologies of two configurations. Table 2-3 shows a weight comparison of the two circuits. The two concepts have basically the same number of circuit elements. The only major component difference is the output capacitor C4. The buck regulator output capacitor only has to filter the ac current in the inductor while the buck-boost output capacitor must supply load current while the transistor switch is ON. As a result, because of the larger size of the capacitor required in the buck-boost circuit the buck regulator will be lighter in weight.

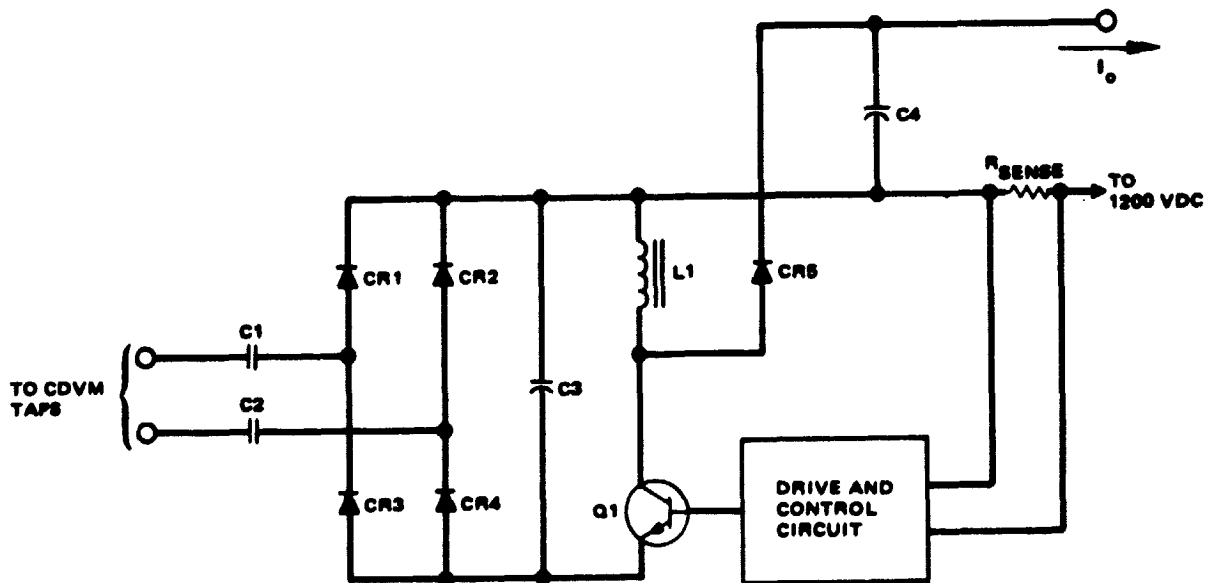


Figure 2-10. Buck-Boost regulator.

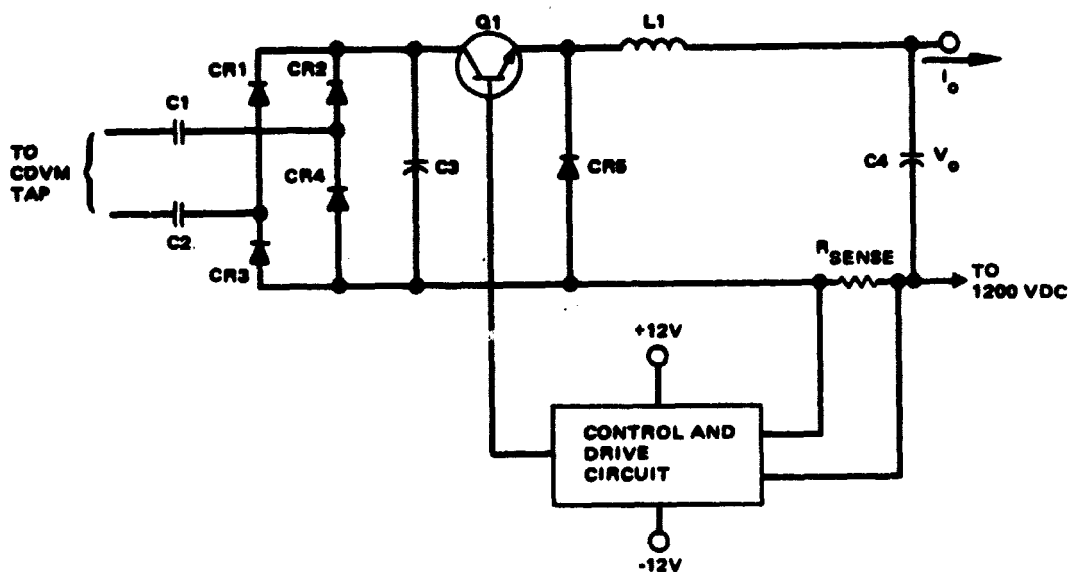


Figure 2-11. Buck regulator.

TABLE 2-3. WEIGHT COMPARISON

	Buck Regulator	Buck-Boost Regulator
	Weight (Grams)	Weight (Grams)
Power Stage		
L1	26 (22 mm pot core)	26 (22 mm pot core)
C1, C2, C3	6 (1 μ f, 150 V)	6 (1 μ f, 150 V)
C4	2 (1 μ f, 150 V)	20 (15 μ f, 150 V)
Q1	13 (2N6579)	13 (2N6579)
CR1	5 (3FF50)	5 (3FF50)
Modulator Circuit		
1 Drive Xfmr	10 (18 mm pot core)	10 (18 mm pot core)
Misc. Circuitry	20	20
± 12 Vdc Supplies		
1/2 Xfmr	8 (14 mm pot core)	8 (14 mm pot core)
Misc. Circuitry	5	5
Total Weight	<u>95 Grams</u>	<u>113 Grams</u>

In addition to less weight as shown in Table 2-3, the buck regulator has a higher efficiency than the buck boost regulator as listed in Table 2-4, which indicates that the buck regulator has an overall advantage. The buck-boost losses will be higher due to the larger currents and voltages associated with the switch transistor Q1 and the commutating rectifier CR5.

TABLE 2-4. EFFICIENCY COMPARISON OF BUCK AND BUCK-BOOST REGULATORS

	Buck Regulator Losses, Watts	Buck-Boost Regulator Losses, Watts
Switching (Q1)	1.22	2.22
Rectifier (CR1 - 4)	0.32	0.32
Transistor Fwd (Q1)	0.08	0.13
Rectifier Fwd (CR5)	0.34	0.45
DCR (L1)	0.21	0.21
Drive Power	0.26	0.26
±12 VDC Power	0.18	0.18
Total Losses	2.61	3.77
Efficiency ($P_o = 26 \text{ W}$)	90.9%	87.3%

Since the buck regulator is more efficient and weighs less, it is clearly the choice for this application.

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3.0 FINAL CIRCUIT DESIGN

Figure 3-1 shows the overall block diagram and Figure 4-9 the complete schematic of the breadboard circuit designed and fabricated to meet the Statement of Work requirements in Appendix B. An 80 kilohertz ac voltage generated by a two phase transistor chopper is fed into two CDVM circuits; one producing +1200 Vdc and the other -350 Vdc. Regulation of the +1200 Vdc supply is performed by a 160 kilohertz boost-add converter which supplies a negative voltage to the transistor chopper. Regulation of the -350 Vdc supply is accomplished by a linear dissipative regulator. Two buck regulator circuits are ac coupled to the +1200 Vdc CDVM circuit to regulate the +0.65 Adc and 0.5 Adc constant current supplies, respectively. An auxiliary dc-dc converter generates ± 12 Vdc bias voltages for the control and drive circuitry in the various supplies.

3.1 TWO-PHASE TRANSISTOR CHOPPER

The two-phase transistor chopper shown in Figure 3-2 operates at 80 kilohertz. During one-half cycle, Q1 and Q4 are driven ON while Q2 and Q3 are held OFF. In the following half cycle Q2 and Q3 are turned ON while Q1 and Q4 are OFF. It is extremely important that Q1 and Q2 (or Q3 and Q4) are never ON at the same time. Since the transistor storage time could represent a large percentage of a half cycle, Baker diode clamps have been employed to prevent the transistors from saturating. The drive transformer uses proportional current feedback windings to provide adequate base drive.

The drive circuit for the chopper is shown in Figure 3-3. A single integrated circuit (Motorola MC 3420) generates the two-phase drive signals as well as providing the 160 kilohertz ramp used in the boost-add pulse-width modulation circuit. The drive voltages to Q1 and Q2 (V_{D1} and V_{D2} ,

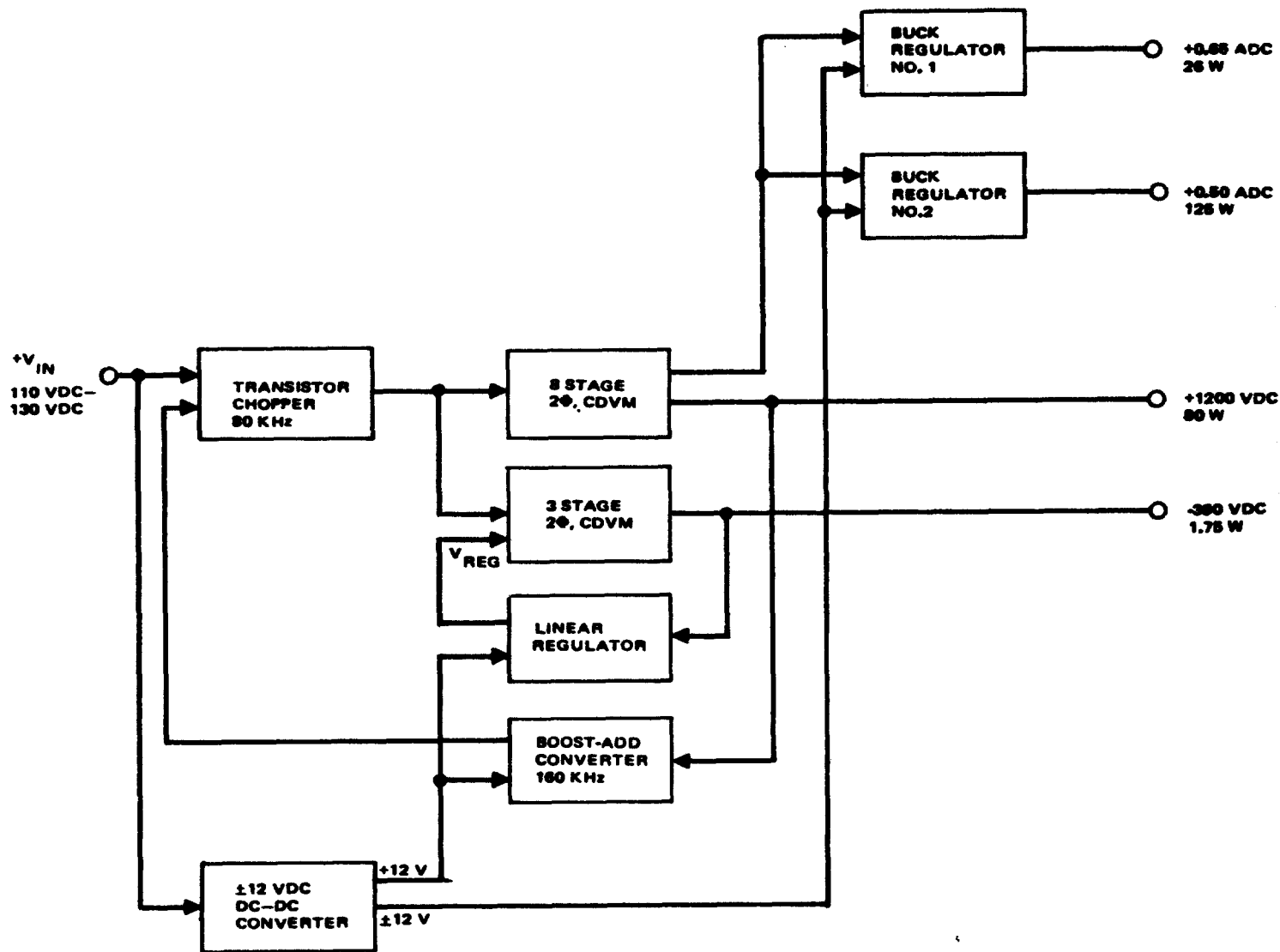


Figure 3-1. Block diagram final breadboard design.

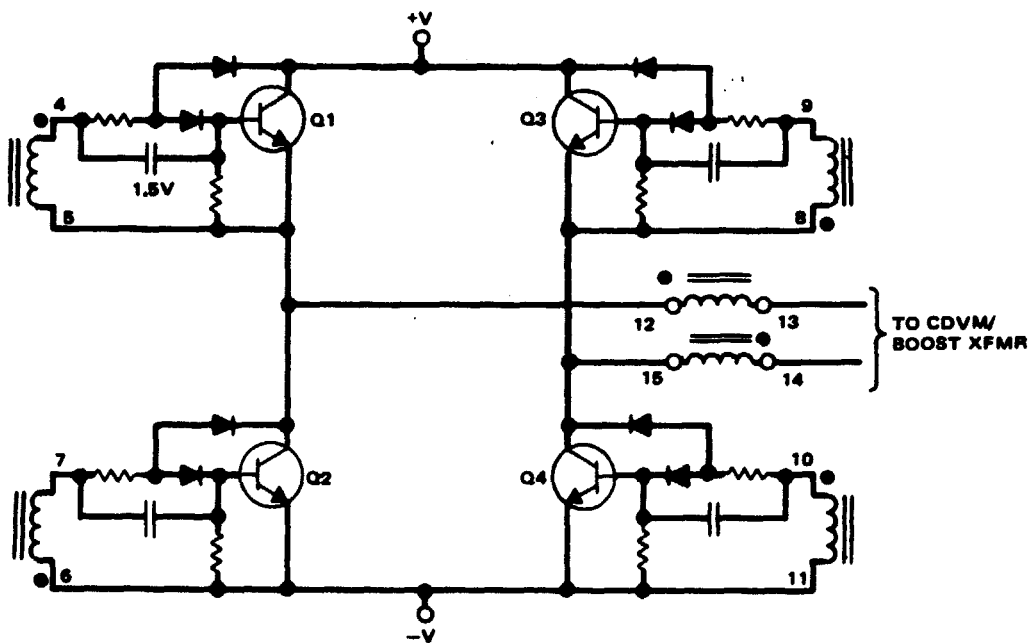


Figure 3-2. Two-phase transistor chopper.

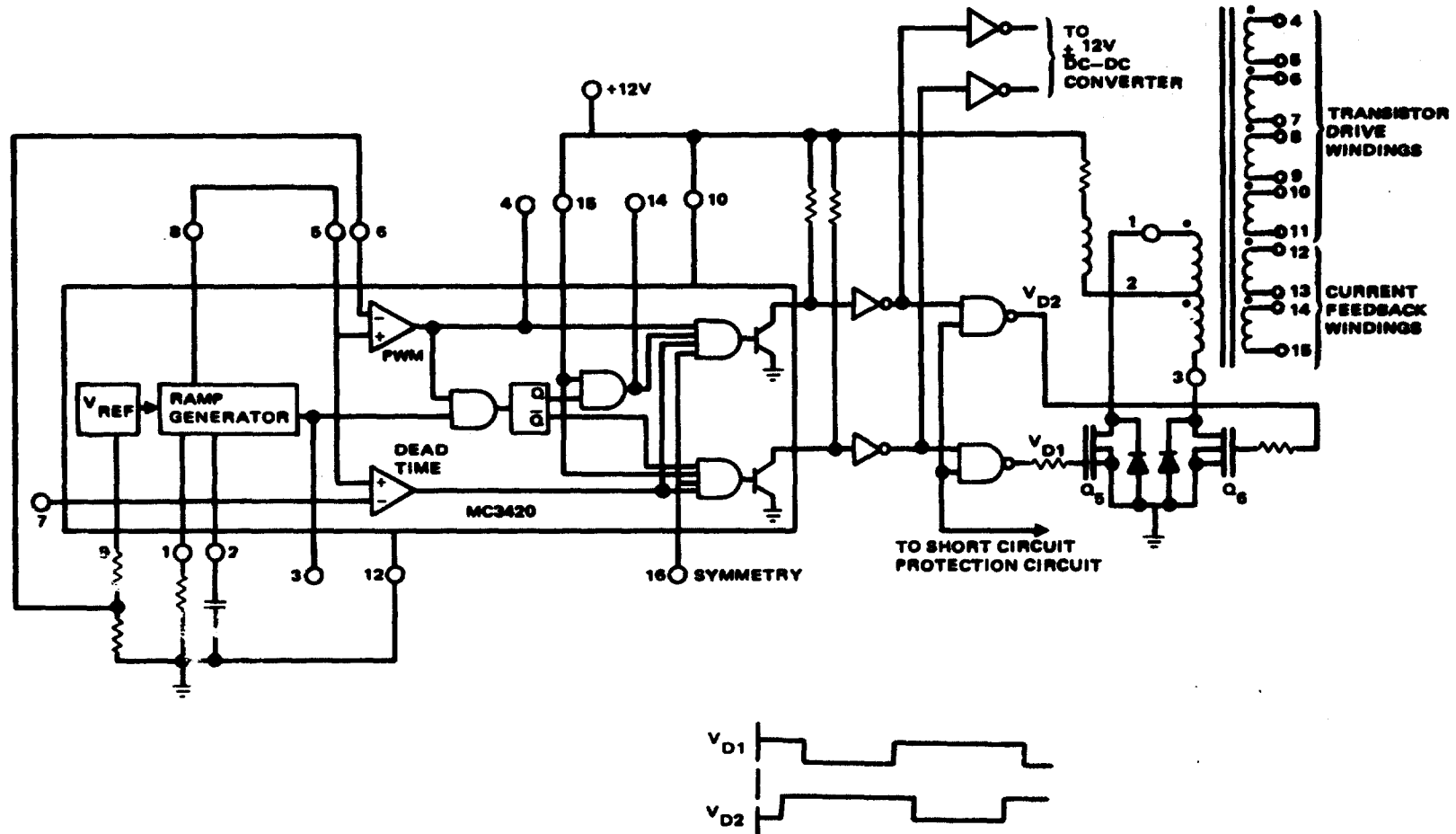


Figure 3-3. Logic and drive circuit.

respectively) are shown. When V_{D1} and V_{D2} are both high, Q1 and Q2 are both turned ON which effectively shorts out the voltage on the drive transformer and turns OFF all four transistors in the two-phase chopper. When only V_{D1} is high, a voltage is applied across the primary of the transformer which causes chopper transistors Q2 and Q3 (Figure 3-2) to be ON. When only V_{D2} is high, Q1 and Q4 of the transistor chopper are turned ON. A signal from the 1200 Vdc overload protection circuitry causes both Q5 and Q6 in Figure 3-3 to be continuously turned ON, turning OFF all transistors in the chopper.

3.2 TWO-PHASE 1200 VDC CDVM

Figure 3-4 shows the two-phase 1200 VDC CDVM including the low voltage tap points referenced to +1200 VDC. Each capacitor in the 8 stage CDVM is a $2\ \mu\text{f}$, 200 V capacitor. The capacitors which ac couple the CDVM voltages to the bridge rectifiers are $1\ \mu\text{f}$, 200 V capacitors. The resistors RS1 and RS2 are used to sense the return currents from the low voltage loads to control the pulse width of the current regulator switches.

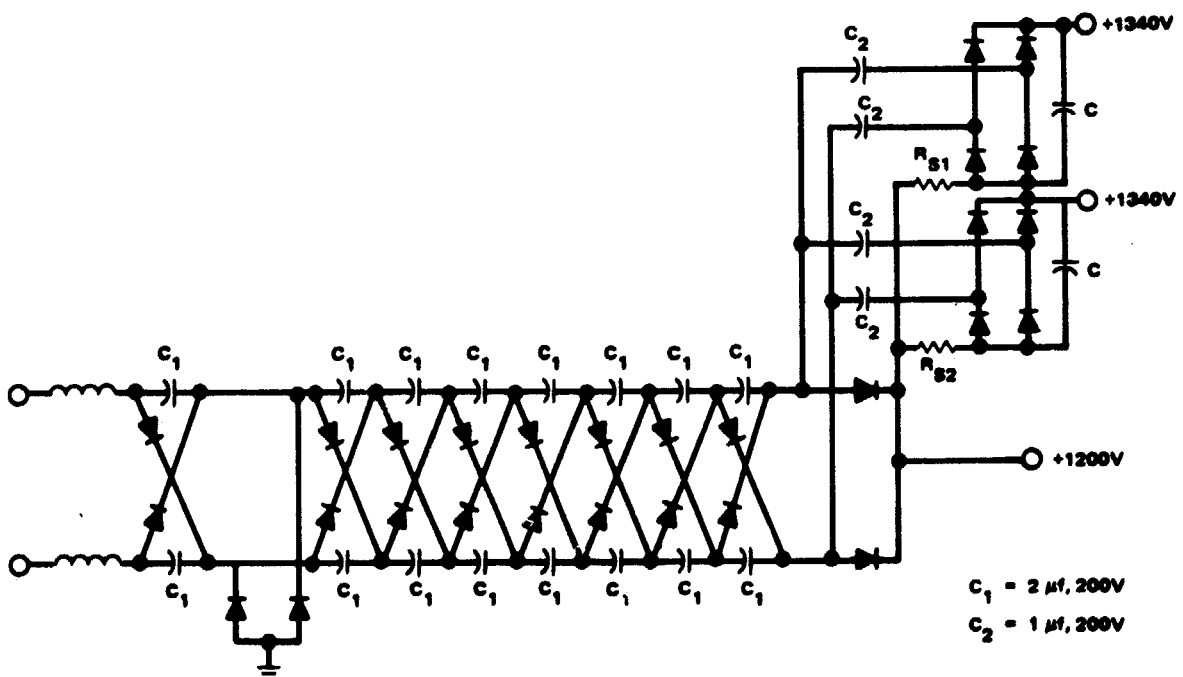


Figure 3-4. +1200 Vdc CDVM including voltage taps.

The 1200 VDC regulator (Figure 3-5) consists of a control amplifier, pulse width modulator, a transformer isolated negative supply and an LC filter which controls the negative supply input to the transistor chopper. If the output voltage is initially above the nominal setpoint, the control circuitry will cause the pulse width to decrease. With the switch, Q1, ON for a shorter period, the average magnitude of the voltage into the LC filter will decrease. The output voltage from the filter will then become less negative resulting in a lower voltage on each capacitor in the CDVM. Finally, the output voltage will be reduced until the error between the dc voltage fed back to the control amplifier and the reference is reduced to zero. A schematic of the control amplifier and pulse-width modulator is shown in Figure 3-6.

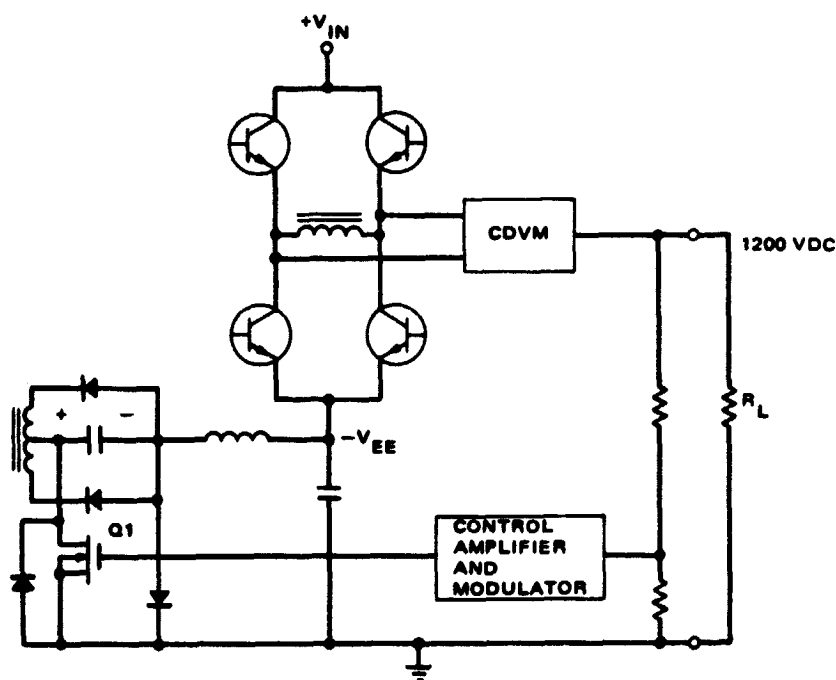


Figure 3-5. 1200 Vdc regulation approach.

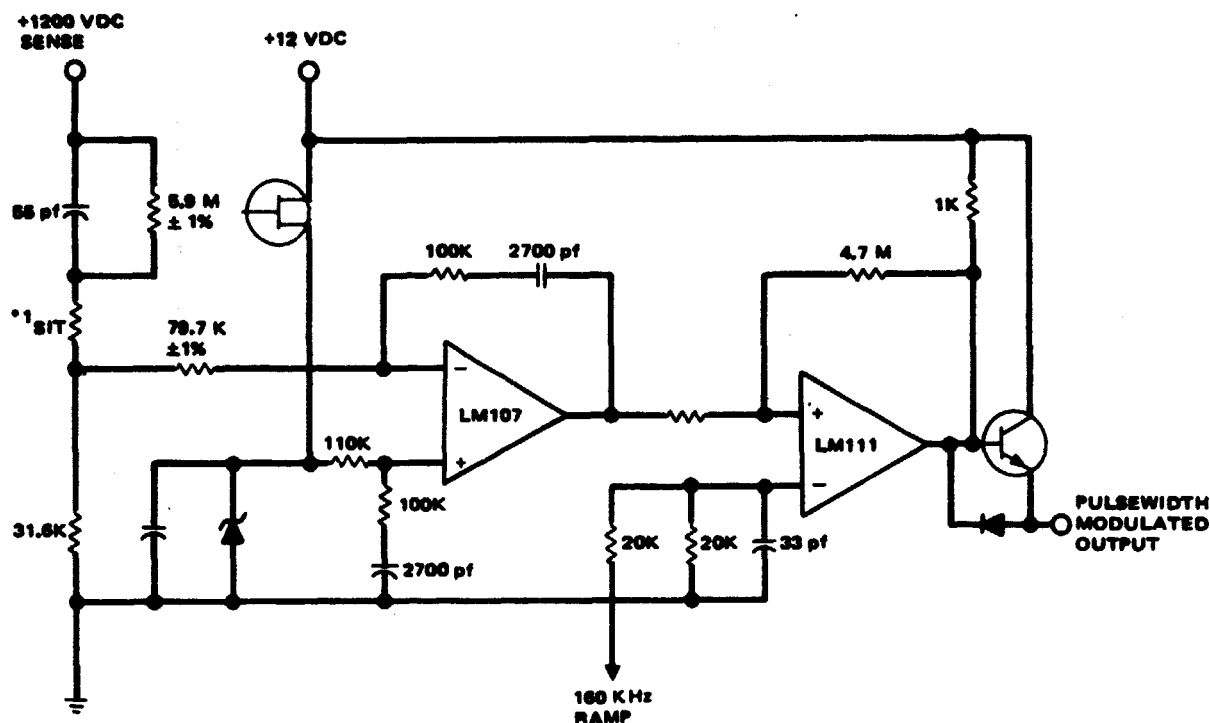


Figure 3-6. Control amplifier and modulator.

As previously described in 2.4, short circuit protection requirements dictate the need for an output inductor and current sensing circuit. The output inductor has been designed to be approximately 0.3 mH during short circuit conditions. The resultant peak current is limited to 46A in the output, or 23A in each rectifier string which is a safe limit for the rectifiers considering the short duration of the current pulse.

A current sensing circuit has been designed as shown in Figure 3-7, which will turn off the drive current to the transistor chopper for approximately 1 ms when an overcurrent occurs on the 1200 Vdc output. The load current is returned to ground through a 2Ω sense resistor, R6. When a load fault occurs, transistor Q1 turns on and discharges the voltage on capacitor C2. When the voltage on C2 falls below the reference voltage (VR1), the output of the comparator U1 goes low and disables the drive circuit. When the load current decays below the trip point, Q1 turns off and C2 begins to recharge. When the voltage on C2 becomes greater than the reference voltage, the drive circuit is allowed to function until the output current again

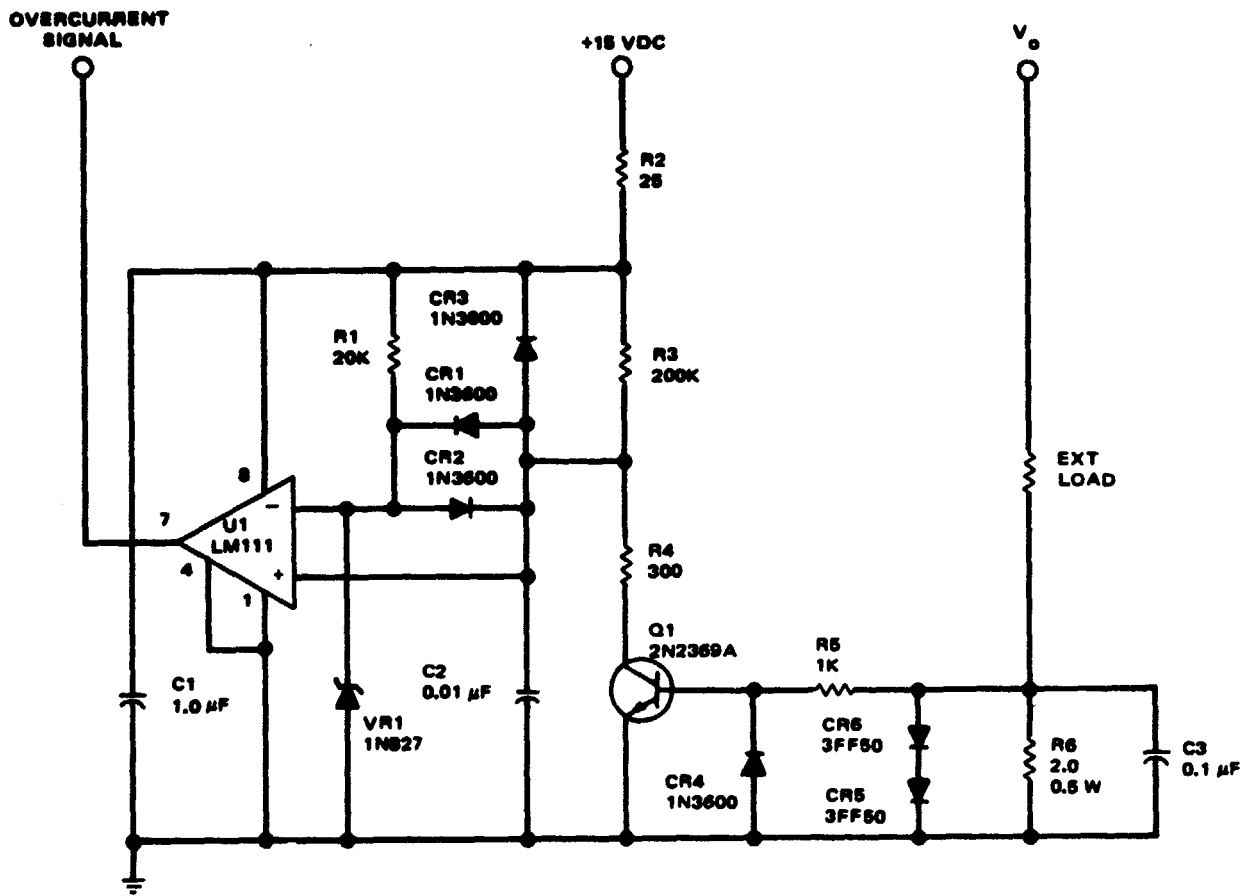


Figure 3-7. Short-circuit sensor.

exceeds the trip point. If the circuit is operating into a continuous short, the circuit will recycle once every millisecond until the short is removed.

3.3 -350 VDC CDVM

The -350 Vdc supply consists of a three stage CDVM and a linear regulator circuit. Figure 3-8 demonstrates the basic regulation technique. The output voltage from the CDVM is equal to the sum of series capacitor voltages and the negative supply voltage. The voltage on the first capacitor stage is equal to the input voltage minus the linear regulator voltage. The

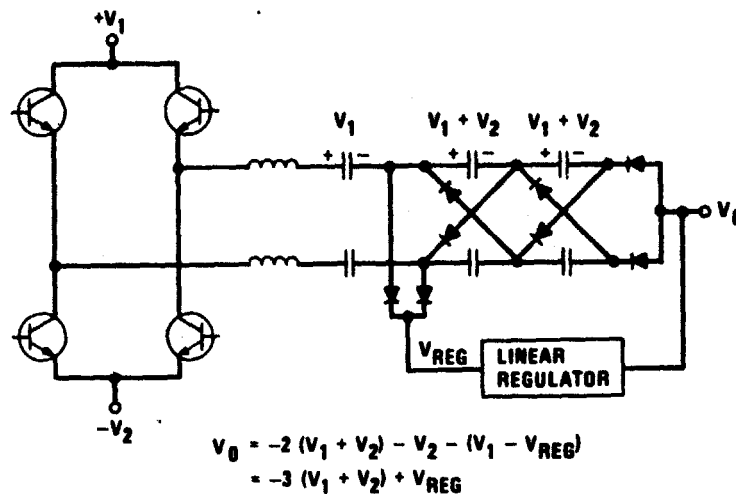


Figure 3-8. -350 Vdc CDVM regulation approach.

capacitors in the following stages have the sum of $V_1 + V_2$ across them. The resultant output voltage is then:

$$V_o = -2(V_1 + V_2) - (V_1 - V_{REG}) - V_1$$

$$= -3(V_1 + V_2) + V_{REG}$$

As V_1 And V_2 vary, the linear regulator adjusts V_{REG} to maintain the constant output voltage. Figure 3-9 shows the details of the regulation circuit.

Short circuit protection is accomplished by L1, L2, and L3. The output inductor, L1, limits the peak instantaneous current during a fault.

It can be shown that if there is a constant short across the -350 Vdc output, the equivalent circuit of Figure 3-10 is applicable. The short circuit output current will be the sum of the linear regulator maximum current (11 ma) plus 1/4 the peak-to-peak ac current in the inductors. As V_2 approaches 0 Vdc, the peak inductor current will approach zero. Therefore, the worst case short circuit current will occur when the negative supply is

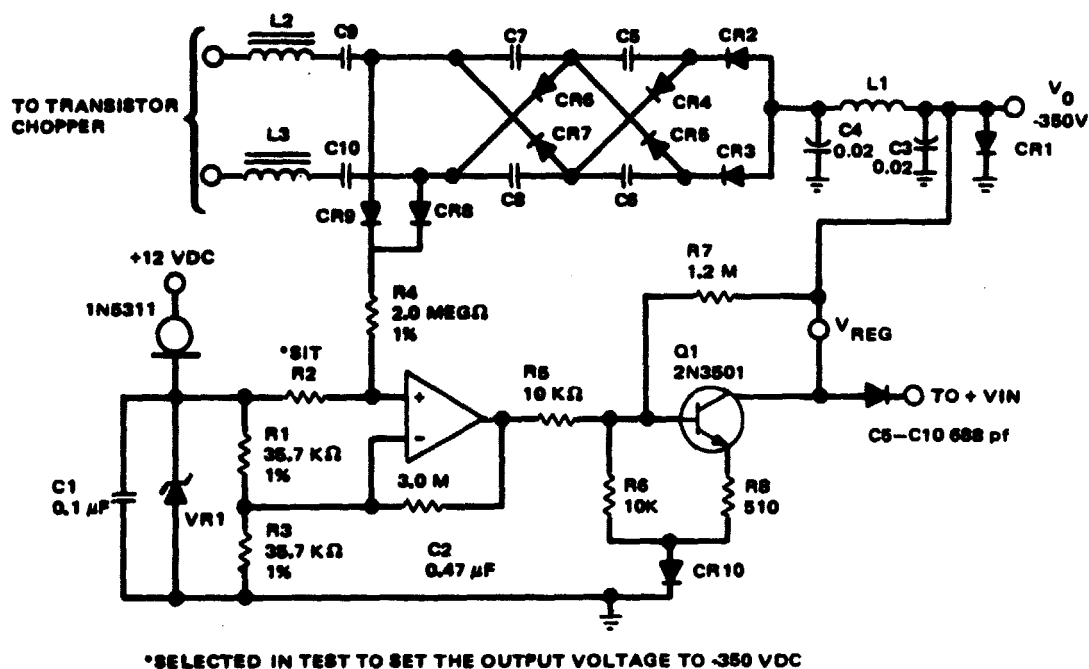


Figure 3-9. -350 Vdc regulator circuit.

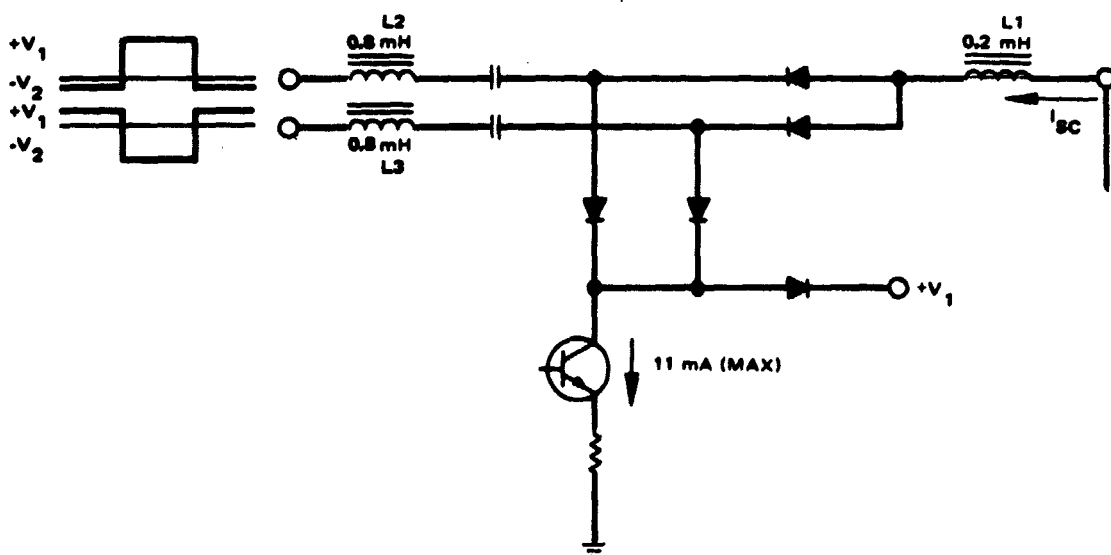


Figure 3-10. Equivalent circuit during an output short (-350 Vdc supply).

operating at its maximum magnitude. The maximum peak-to-peak inductor current is approximately

$$\begin{aligned}
 I_{L(p-p)} &= \frac{0.5 V_{2(\max)}}{L} t_{on} \\
 &= \frac{0.5 (40)}{1.0 \times 10^{-3}} \frac{1}{80 \times 10^3} \frac{1}{2} \\
 &= 0.125 \text{ A}
 \end{aligned}$$

The total short circuit current is then

$$\frac{1}{4} I_{L(p-p)} + 0.011 \text{ A} = 0.042 \text{ Adc}$$

Therefore, if a continuous fault occurs, inductors L2 and L3 limit the output current to an acceptable level.

3.4 BUCK REGULATOR CIRCUIT

Two current-regulated supplies are referenced to the +1200 Vdc output. These supplies are identical buck regulators with current ranges of 0.10 to 0.50 Adc and 0.10 to 0.65 Adc. The buck regulators are capacitively coupled to the CDVM as previously discussed in 2.4.

As shown in Figure 3-7, the current sense resistor, R_6 , has essentially the same current flowing through it as the filter inductor, assuming that the currents in the control circuitry sensing lines are insignificant. If the regulator circuit causes the average inductor current to remain constant, the load current will be constant. The output capacitor will filter the ac component of the inductor current so that the load current will be primarily dc.

The buck regulator control and drive circuitry is shown in Figure 3-11. The control amplifier U1 compares the voltage across the sense resistor, R10, to an adjustable reference voltage across R11. The control amplifier output is buffered by a transistor, Q1, which prevents the input to the comparator, U2, from going below the signal return. Since the ramp input to

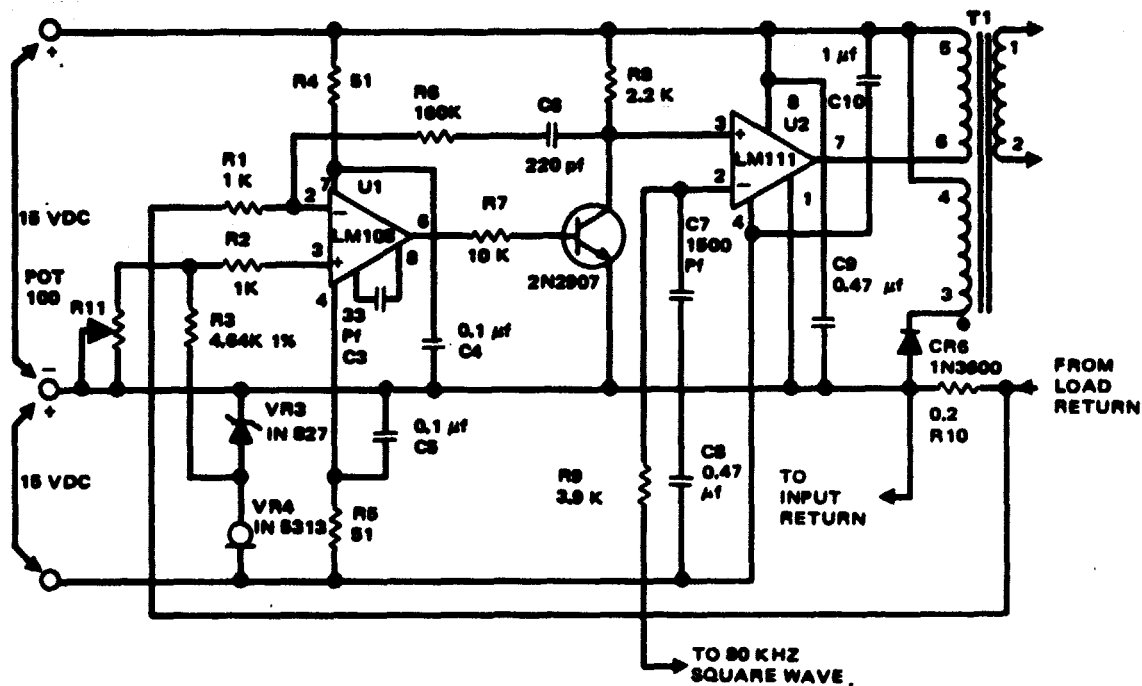


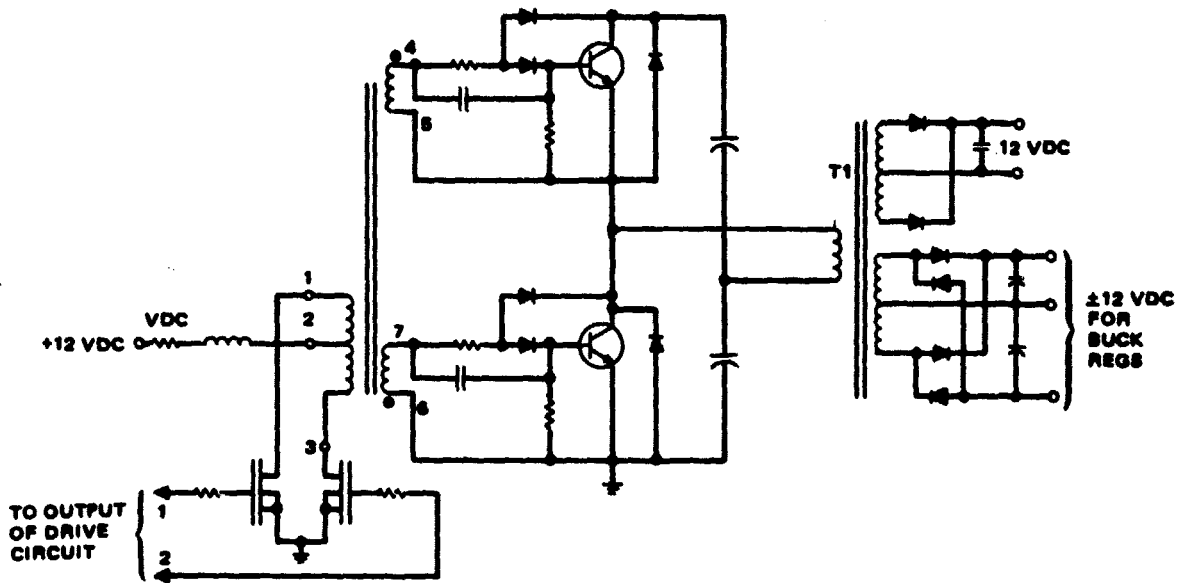
Figure 3-11. Buck regulator control and drive circuit.

U2 swings symmetrically about the signal return, the maximum duty cycle will be 50 percent. As a result of the comparison between the control amplifier output and ramp, U2 produces a pulse width modulated signal which is used to drive the transistor switch through the drive transformer, T1.

Short circuit protection is easily accomplished since the supply already regulates current. As long as the circuit responds rapidly enough to prevent large transient currents in the transistor, no additional short circuit protection is required. In this particular application, the response of the control circuit will prevent the transistor current from exceeding 1.0 A during a load fault.

3.5 ± 12 V DC-DC CONVERTER

Two isolated 12 Vdc supplies are required to provide bias power for ground referenced supplies and 1200 Vdc referenced supplies. Total power requirement are approximately 3 watts. Figure 3-12 is a simplified schematic of the ± 12 Vdc dc-dc converter. The drive signal generator



(Figure 3-3), operating at 80 kilohertz drives the circuit. One of the +12 Vdc supplies is referenced to ground and provides bias power for the +1200 Vdc drive and regulator circuits and the -350 Vdc regulator circuit. The ± 12 Vdc outputs are referenced to +1200 Vdc and provide bias power for the two buck regulator circuits.

Each of the supplies are capable of withstanding a continuous short across the output terminals. However, the converter must also survive when any output terminal is shorted to output return or any two outputs are shorted together. Figure 3-13 demonstrates the added circuitry necessary to protect for these various modes.

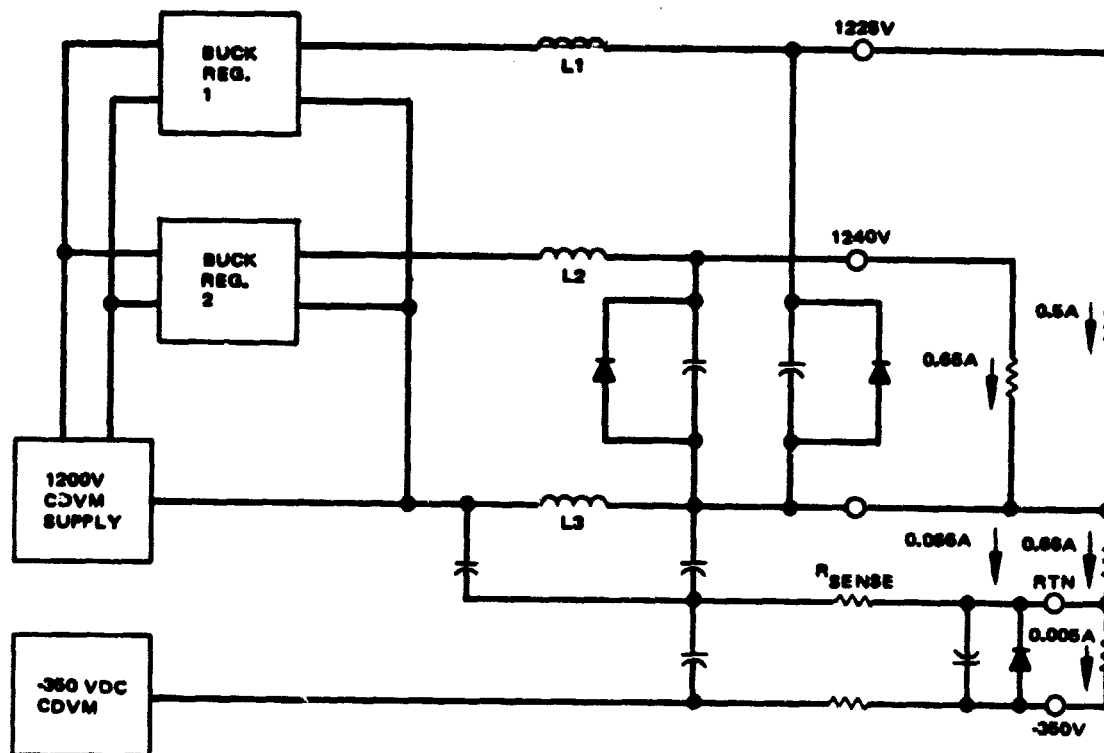
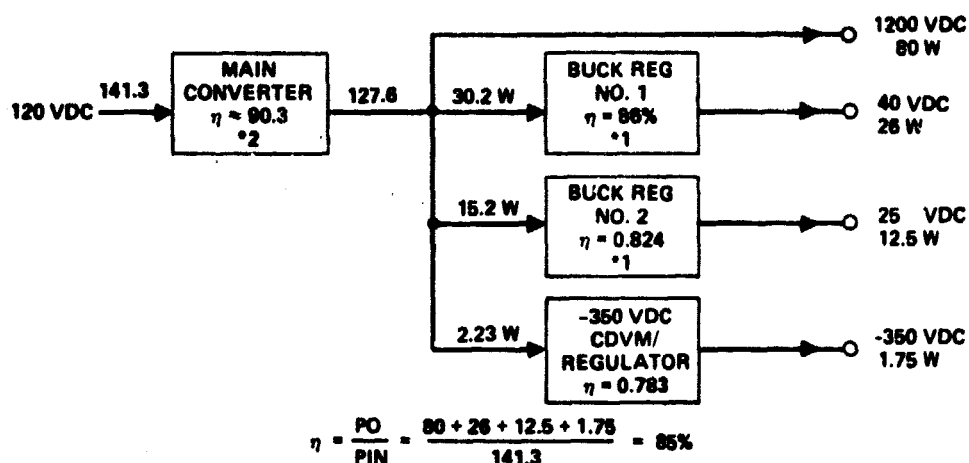


Figure 3-13. Short circuit protection.

all of the components. A short from either the buck regulator output or from the 1200 Vdc output to the -350 Vdc supply causes the rectifier across the -350 Vdc output capacitor to be forward-biased, routing the short circuit current through the 1200 Vdc current sense resistor.

3.7 CONVERTER EFFICIENCY

The overall efficiency of the converter at 120 Vdc input and full load is calculated using the model of Figure 3-14. The main converter consists of the 12 Vdc dc-dc converter, two-phase transistor chopper, +1200 Vdc CDVM, and boost-add regulation circuits. The power processed by the other supplies must first be processed by the main converter. The projected efficiency based on the model was 85 percent.



*1 INCLUDES LOSSES IN SHORT CIRCUIT PROTECTION INDUCTORS
 *2 PROJECTION OF PERFORMANCE REPORTED IN REPORT NO. CR-135309

Figure 3-14. Efficiency calculation block diagram.

The main converter (except for the ± 12 Vdc inverter) was previously developed on a former NASA contract⁵. Figure 3-15 summarizes efficiency measurements made on the original engineering breadboard designed and fabricated on the previous contract. From this curve, the efficiency for processing 100 watts at 120 Vdc input was approximately 91 percent. Measurement of the same basic supply after adding the separate ± 12 Vdc

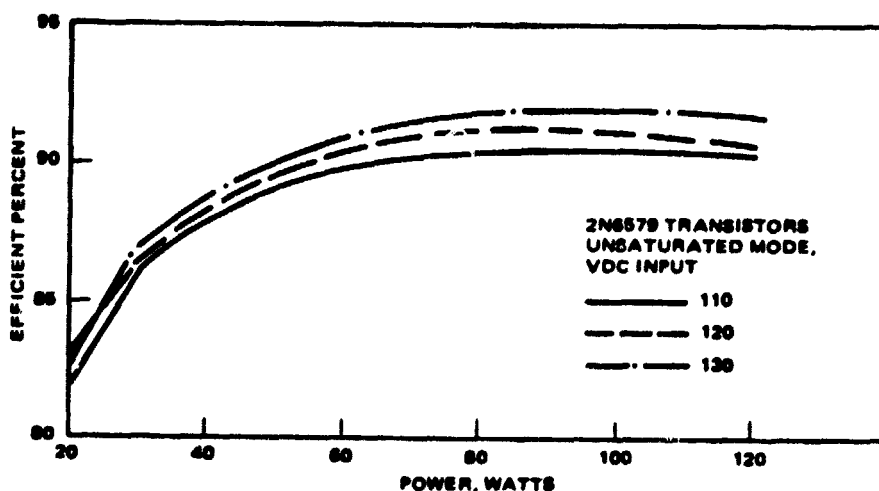


Figure 3-15. Efficiency of CDVM power supply.

DC-DC converter and some additional fault protection circuitry resulted in an efficiency of 90.3 percent.

The projected buck regulator efficiency for the two cases is summarized in Table 3-1 with the applicable equations used to calculate the losses given in Appendix A.

TABLE 3-1. BUCK REGULATOR POWER*
DISSIPATION SUMMARY

	Symbol	12.5 W, 0.50 A Supply, Watts	26W, 0.65 A Supply, Watts
Switching (Q1)	P_{SW}	0.84	1.09
Rectifier (CR1 - 4)	$P (CR1 - 4)$	0.21	0.44
Transistor Fwd (Q-1)	P_{FWD}	0.09	0.19
Rectifier Fwd (CR5)	$P (CR5)$	0.10	0.16
DCR (L1)	P_{L1}	0.12	0.21
Drive Power	P_D	0.13	0.26
±12 Vdc Power	P_{BIAS}	0.18	0.18
SC Inductors**	P_{DCR}	1.00	1.69
	Total	2.67	4.22
	Efficiency	82.0%	86.0%

* Does not include additional losses in the main bridge or CDVM.
 *** Test data from breadboard.

The losses associated with -350 Vdc CDVM and regulator (excluding losses in the transistor chopper) and main bridge circuit are summarized in Table 3-2. The linear regulator contributes the largest single loss term.

TABLE 3-2. CDVM AND MAIN BRIDGE
DISSIPATIONS

+12 Vdc Bias Power	0.072 W
Voltage Sense Divider	0.062 W
Reg Transistor (Q1)	0.350 W
Total	<u>0.484 W</u>
$\eta = \frac{1.75}{1.75 + 0.484} = 78.3\%$	

In general, $V_1 + V_2$ is approximately 140 Vdc. The transistor (Q1 of Figure 3-9) must then support 70 Vdc ($3 \times 140 = 350$ Vdc) with 5 ma flowing through it. Because of the low output current (0.005 A max.) the losses in the CDVM rectifiers and capacitors are not very significant and have been ignored.

4.0 BREADBOARD FABRICATION AND TEST RESULTS

A breadboard was fabricated using the circuit design described in Section 3. Careful layout of the individual circuit cards in the final assembly was required to avoid potential noise problems. Figure 4-1 is a photograph of the deliverable assembly, and Figure 4-9 at the end of this section is the complete schematic. Following assembly, the breadboard was extensively tested to demonstrate conformance with the design requirements. The data and results are described below under appropriate headings.

4.1 TEST SETUP

Figure 4-2 shows the test setup used to measure the efficiency and regulation of the CDVM converter. When using a digital voltmeter to measure input power, it is necessary to filter out the high frequency ripple to prevent erroneous data. A 3.2 mh inductor and a 6000 μ f electrolytic capacitor input filter were used during efficiency and regulation tests.

All shunts were initially checked by putting a test current through all three shunts simultaneously and measuring the voltage across them. It was found that the shunt voltages were accurate to within 0.1 percent of the expected values, based on the respective ratings.

The test equipment types are summarized in Table 4-1. Transient response measurements used a Tektronix 7000 series oscilloscope and a Tektronix P6042 DC current probe. Transient load tests used either a high voltage relay or a knife switch to connect a resistor in parallel with the minimum load.

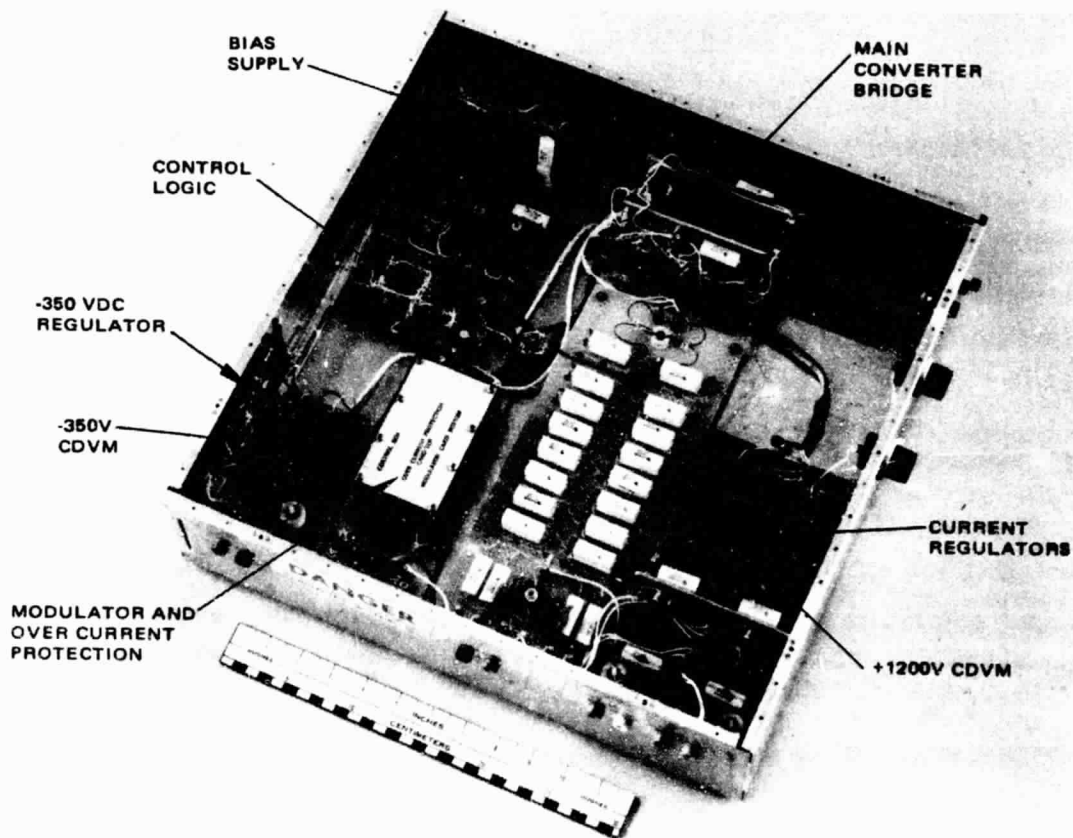


Figure 4-1. Photograph of breadboard.

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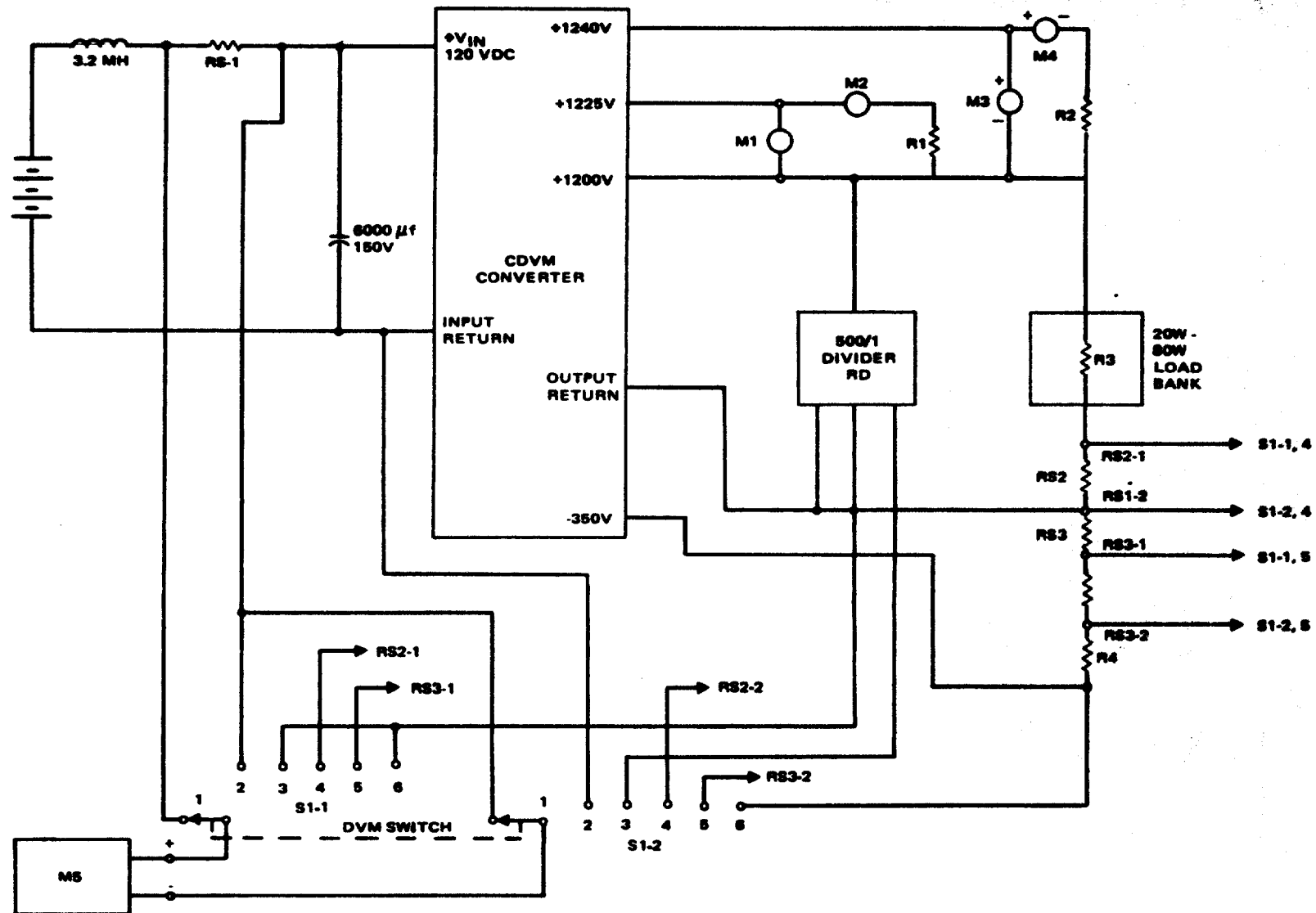


Figure 4-2. Setup for efficiency/regulation tests.

TABLE 4-1. TEST EQUIPMENT LIST

M1	Polyranger Model C Combination 4C
M2	Polyranger Model C Combination 4C
M3	Polyranger Model C Combination 2C
M4	Polyranger Model C Combination 2C
M5	Hewlett Packard, Model 3460B
R _{DIV.}	John Fluke Mfg. Model 80E
R _{S1}	2A, 50 mV Shunt (± 0.5 percent)
R _{S2}	0.5000 ± 0.1 percent Shunt Resistor
R _{S3}	2.000 ± 0.1 percent Shunt Resistor

4.2 EFFICIENCY

Resistive loads were connected across the four outputs to obtain the nominal power dissipation at nominal voltages or currents. In the case of the two current supplies which were biased off ground, less precise analog meters which could have both terminals high with respect to ground had to be used instead of digital meters, resulting in less accurate calculation of power dissipation.

Current and voltage readings for both inputs and outputs were taken, and their respective products gave the values of power input and power output, for three input voltages as shown in Table 4-2. The overall efficiency is essentially constant at 84 percent which is slightly less than the design objective of 90 percent given in Appendix B.

TABLE 4-2. EFFICIENCY AT RATED LOAD

VIN	PIN	POUT	η
110.0 VDC	144.1 W	121.0 W	84.0%
120.0 VDC	143.0 W	120.9 W	84.5%
130.0 VDC	142.7 W	120.8 W	84.6%

4.3 REGULATION

Table 4-3 shows the ΔV_o or ΔI_o for minimum to maximum load changes, and the calculated percent change. No change in voltage or current, respectively was measured for the +1200 V and 0.65 A supplies. The -350 Vdc supply, which uses a dissipative regulator shows the maximum of 0.92 percent change for a 5 to 1 load change. A 2.5 change of load produce a 0.6 percent change in the 0.5 Adc constant current supply; although not tested, it could be assumed that a larger load variation would result in a greater output current change, but still well within specification requirements.

At constant load, the output voltage/current changes of the four supplies were measured at the nominal input of 120 V and ± 10 V variations. The results are shown in Table 4-4. Here only the two current supplies employing buck regulators showed any significant changes.

In summary, the 1200 Vdc supply output changes were less than 0.1 percent for line and load variations. The -350 Vdc supply was insensitive to line changes but varied approximately 0.9 percent from minimum load to full load. Both buck regulator outputs varied by less than 1.7 percent for line and load variations. The supply met all of the specification requirements for regulation.

4.4 RIPPLE VOLTAGE/CURRENT

Figure 4-3 shows the ripple on the 1200 V output with the buck regulators operating at full load and turned off. The 1200 V output alone has a 5 V pp, nominal second harmonic of 200 kHz ripple, increasing to 12 V pp

TABLE 4-3. OUTPUT CHANGES WITH RESPECT TO LOAD CHANGES

Supply	ΔP_L	ΔV_o or ΔI_o	% Change
1200 Vdc	20 W - 80 W	0.0 V	0.0%
-350 Vdc	0.35 W - 1.75 W	3.25 V	0.92%
+0.65 Adc	24.7 W - 28.6 W	0.000 A	0.0%
0.50 Adc	5 W - 12.5 W	0.003 A	0.6%

TABLE 4-4. OUTPUT CHANGES WITH RESPECT TO
INPUT VOLTAGE CHANGES

V_{IN}	1200 Vdc Output Voltage	-350 Vdc Output Voltage	0.65A Output Current	0.5A Output Current
110 Vdc	1200.3 Vdc	-352.7 Vdc	0.649 Adc	0.502 Adc
120 Vdc	1200.4 Vdc	-352.7 Vdc	0.649 Adc	0.505 Adc
130 Vdc	1200.4 Vdc	-352.7 Vdc	0.652 Adc	0.500 Adc
Maximum Output Changes	0.1 Vdc	0.0 Vdc	0.003 Adc	0.005 Adc
% Change	0.00%	0.00%	0.46%	1.00%

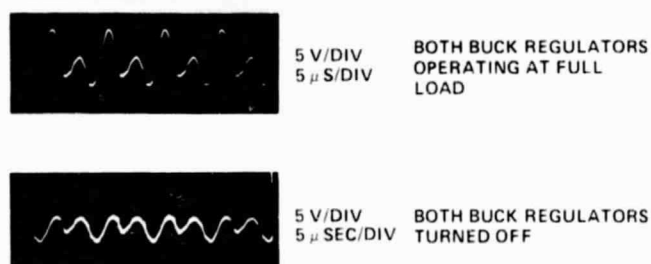


Figure 4-3. 1200 Vdc output ripple
voltage.

with both buck regulators operating at full load. Also both curves can be seen to have a high frequency noise burst occurring every half cycle of the fundamental 100 kHz oscillator frequency. The peak-to-peak amplitude to this noise burst seems to increase in proportion to the increase of 200 kHz ripple.

Ripple on the outputs of both buck regulators is shown in Figure 4-4. The second harmonic amplitude is very low, but the noise bursts from the 1200 V supply, to which these buck regulators are referenced to, appear

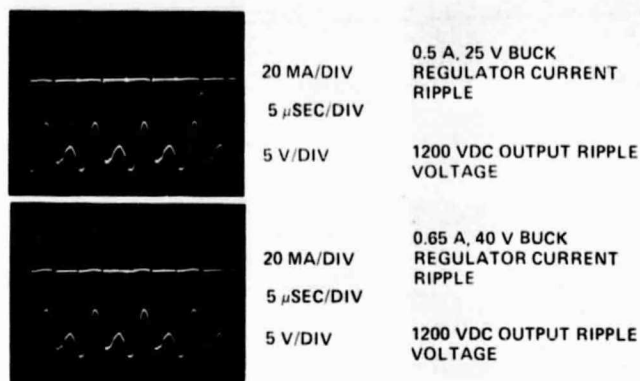


Figure 4-4. Buck regulator ripple current.

to be about 10 mA pp, which is somewhat greater than the 1 percent of full load current specified. Time did not allow the determination of the source of these noise bursts, which appear to be an anomaly rather than an inherent characteristic of the multiple output CDVM being investigated.

4.5 TRANSIENT RESPONSE

Measurements of the transient response of each of the power supplies were made for step application and removal of maximum load to the minimum load, at minimum and maximum input voltages, respectively. For example, making a step change in load from 80 W to 20 W on the 1200 V supply with 130 V applied. Figure 4-5 shows a transient peak of 15 V, at 0.4 millisecond with a total duration of the transient of 1.6 milliseconds before the voltage level returned to nominal. No overshoot appears, indicating that the regulator is overdamped. A step application of load of an identical range, at 110 Vdc input, caused a 12 V drop transient of similar waveform as above.

Figure 4-6 for the -300 Vdc supply shows about a 5 volts change in the amplitude due to step changes in load between 1.78 and 0.35 watts. The settling time is about half that of the 1200 V supply, estimated to be about 0.8 milliseconds, but is appreciably underdamped as can be seen by the series of overshoots.



5 V/DIV
0.2 MS/DIV

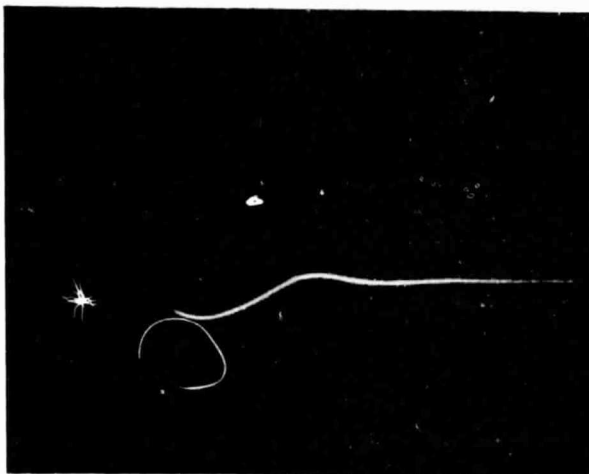
VIN = 130 VDC
 $\Delta PL = 80 \text{ W TO } 20 \text{ W}$



5 V/DIV
0.2 MS/DIV

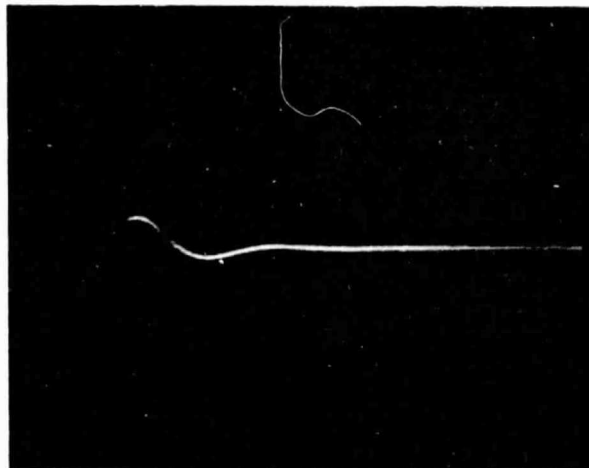
VIN = 110 VDC
 $\Delta PL = 20 \text{ W TO } 80 \text{ W}$

Figure 4-5. 1200 Vdc transient response.



5 V/DIV
0.2 MS/DIV

VIN = 130 VDC
 $\Delta PL = 1.78 \text{ W TO } 0.35 \text{ W}$



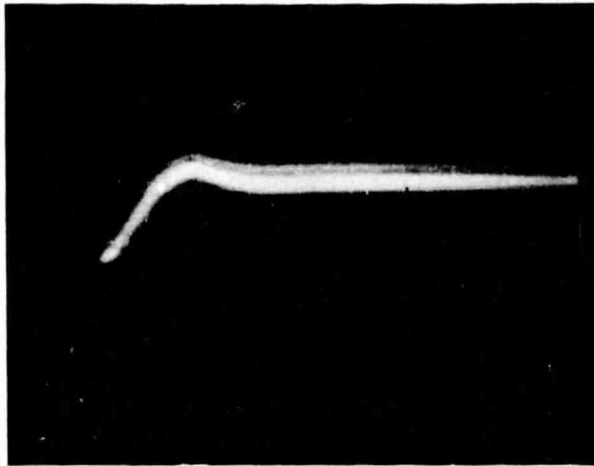
5 V/DIV
0.2 MS/DIV

VIN = 110 VDC
 $\Delta PL = 0.35 \text{ W TO } 1.78 \text{ W}$

Figure 4-6. -350 Vdc transient response.

The 0.5 A transient responses for step coverage in load resistances are shown in Figure 4-7. For a 2.5 step change in load, the transient response is underdamped settling in about 0.8 millisecond.

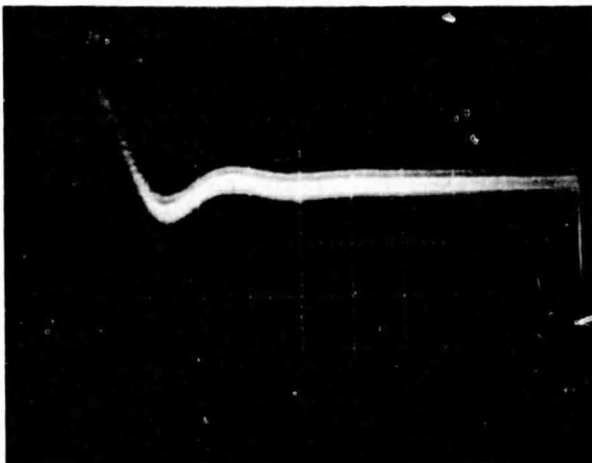
A much smaller step load change, about 16 percent, was applied to the 0.65 A buck regulator, with the response waveforms shown in Figure 4-8. Although difficult to read through the noise, it appears that the response is slightly underdamped. Whether or not a larger change would reveal a definite underdamped condition was not determined.



I_{LOAD}
0.1 A/DIV
0.2 MS/DIV

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$V_{IN} = 110 \text{ VDC}$
 $\Delta P_L = 5 \text{ W TO } 12.5 \text{ W}$



I_{LOAD}
0.1 A/DIV
0.2 MS/DIV

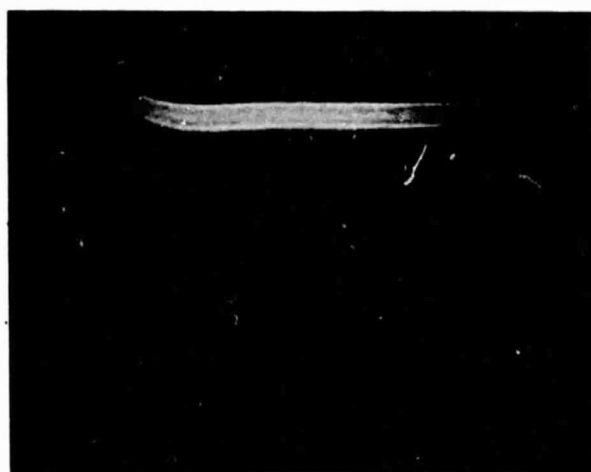
$V_{IN} = 130 \text{ V}$
 $\Delta P_L = 12.5 \text{ W TO } 5 \text{ W}$

Figure 4-7. +25, 0.5A buck regulator transient response.



IL
0.5 A/DIV
0.2 MS/DIV

$V_{IN} = 110 \text{ VDC}$
 $\Delta P_L = 24.7 \text{ W TO } 28.6 \text{ W}$



IL
0.5 A/DIV
0.2 MS/DIV

$V_{IN} = 130$
 $\Delta P_L = 28.6 \text{ W TO } 24.7 \text{ W}$

Figure 4-8. +40 Vdc, 0.65A buck regulator transient response.

The concern of damping in regulators is that certain types of continuing load changes could cause an oscillatory condition to occur which would be highly undesirable. Load dynamic characteristics must be taken into account when matching a multi output power supply to an interrelated load system.

4.6 WEIGHT SUMMARY

The final component weight summary shown in Table 4-5, is 527 grams (1.2 lbs). The two buck regulator supplies are 77 gms each which is less than the specification requirement of 80 gms. The weight of the 1200V CDVM will be 83 gms less if the higher density capacitors, and MJ7161 transistors rather than the 2N6579 transistors are used. The original design was based on these two components but anticipated procurement delays necessitated substitution of commercially available ones.

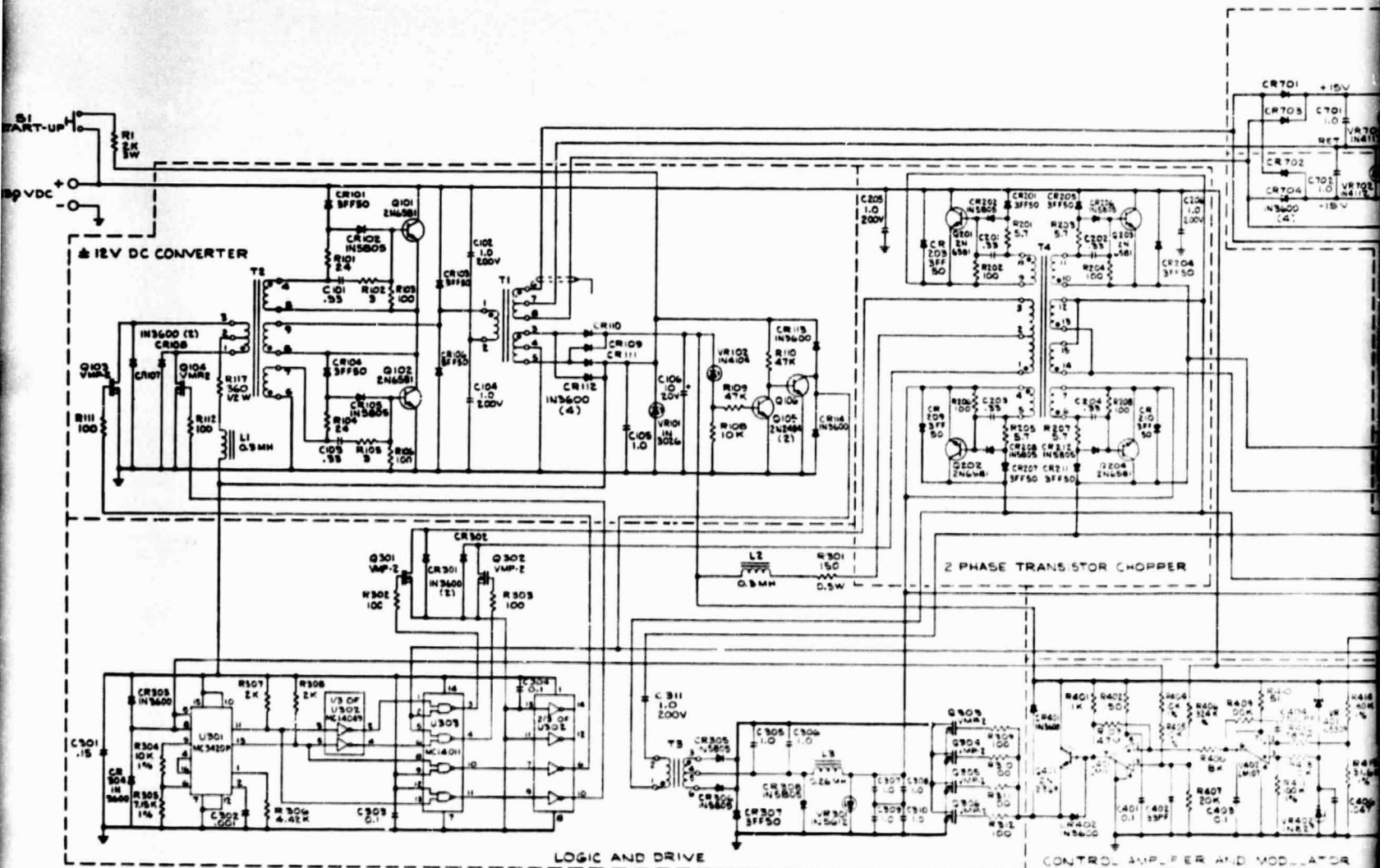
TABLE 4-5. FINAL COMPONENT WEIGHT SUMMARY

1.	1200 Vdc Supply		
	*CDVM	94.6	
	**Bridge	68.2	
	Drive	25.4	
	Boost	43.2	
	Control and Short Circuit Protection	18.2	
			249.6
2.	-350 Vdc Supply		
	CDVM	22.4	
	Regulator	5.6	
	Short Circuit Protection	18.2	
			46.2
3.	Buck Regulator Supplies	77.4	
		X2	154.7
4.	12 Vdc Inverter		76.4
	Total		526.9
*Weight is based on commercially available capacitors. weight = 57.3 grams			
**Uses 2N6579 transistors rather than MJ7161. weight = 26 grams			

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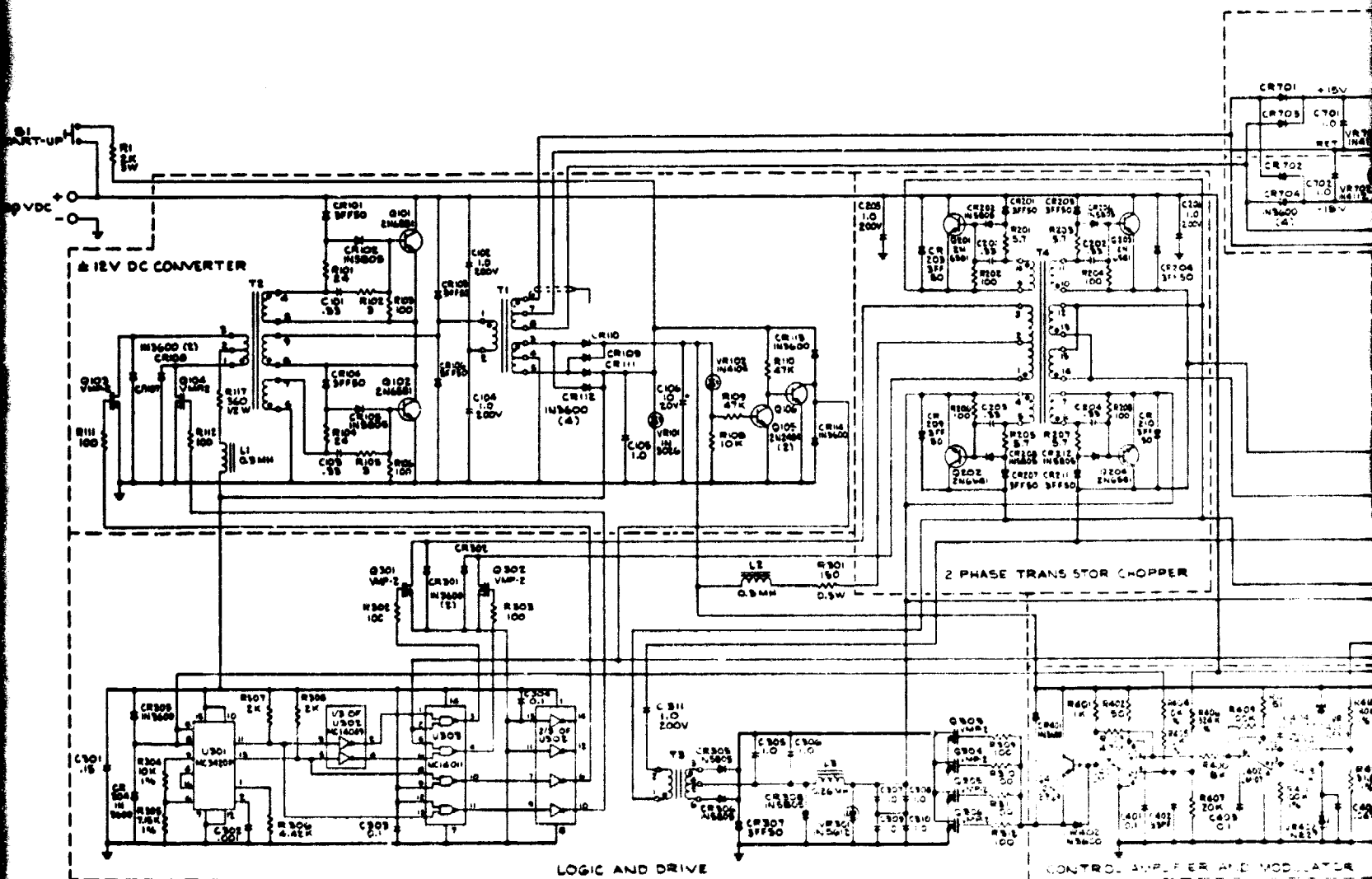
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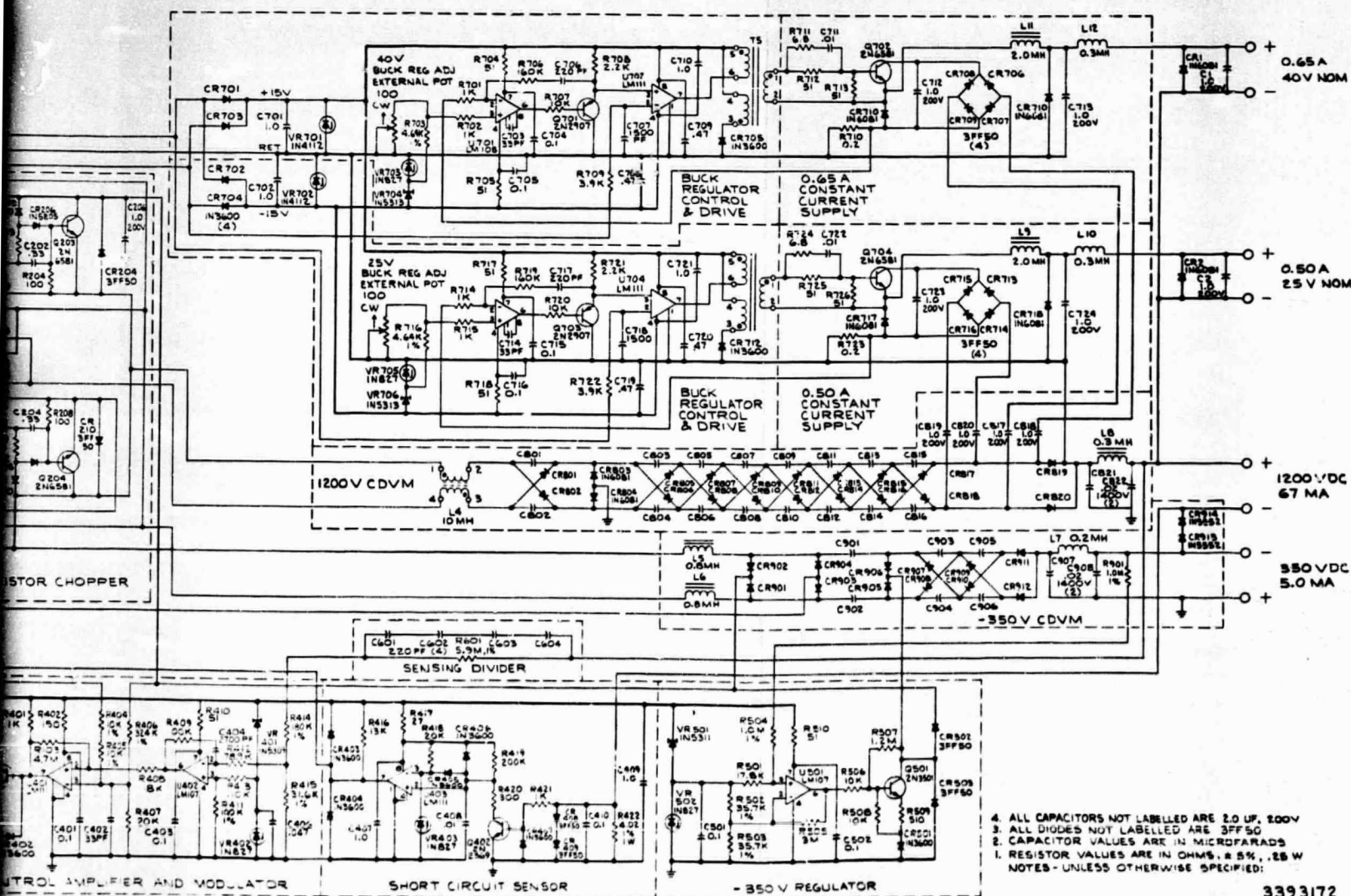


Figure 4-9. Complete schematic of CDVM breadboard.

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5.0 POWER PROCESSOR ASSESSMENT

A study was performed to compare the multi-output CDVM power supply operating a 100 kHz with an existing 8 cm ion engine power processor unit (PPU) designed for 10 kHz. Table 5-1 lists the nine outputs of the 8 cm ion engine PPU. The breadboard CDVM fabricated under this contract had outputs similar to the last four supplies: screen, accel., main discharge, and neutralizer keeper. However, ion engine operating procedures impose additional constraints; for example, it is necessary to turn on the main discharge and neutralizer keeper supplies before turning on the screen and accel., supplies. With the breadboard design, all four supplies came on simultaneously. Figure 5-1 and 5-2 show the partial block diagrams of the existing PPU design and a CDVM based PPU design, respectively, which perform similar functions and can be turned on sequentially as required by the ion engine.

5.1 PPU DESIGN CONSTRAINTS

The existing PPU design has an input filter which filters the 70 Vdc input power. The output of the filter feeds a line regulator, screen supply and discharge supply. The line regulator, a buck type, supplies 48 Vdc power to the distribution inverter which in turn supplies 96 Vac 10 KHz power to the main keeper, accel., and various mag amp/saturable reactor supplies (not shown). The screen and discharge supplies are pulse-width modulated transformer coupled dc-dc converters. The main keeper is a mag-amp, current regulated supply.

TABLE 5-1. 8 cm THRUSTER POWER PROCESSOR SUPPLY SPECIFICATIONS

Supply	Maximum Power	Nominal Power	Regulation, V or I & $\pm\%$	Output Reference Potential	Type Control Input
1. Main vaporizer	6 V at 3 A	5 V at 2 A	I, 5	Spacecraft	1 variable reference
2. Main cathode heater	8 V at 4 A	6 V at 3 A	I, 5	Screen	8 setpoints
3. Main keeper	25 V at 0.5 A	15 V at 0.36 A	I, 3	Screen	4 setpoints
4. Neutralizer vaporizer heater	4 V at 2 A	2 V at 1 A	I, 5	Spacecraft	1 variable reference
5. Neutralizer cathode heater	8 V at 4 A	6 V at 3 A	I, 5	Neutralizer common	8 setpoints
6. Neutralizer keeper	25 V at 0.5 A	20 V at 0.36 A	I, 3	Neutralizer common	4 setpoints
7. Main discharge	42 V at 0.65 A	40 V at 0.5 A	I, 3	Screen	1 variable reference
8. Screen	1200 V at 0.065 A	1180 V at 0.055 A	V, 1	PPU common	Single setpoint
9. Accel.	-350 V at 0.005 A	-300 V at 0.001 A	V, 1	PPU common	Single setpoint

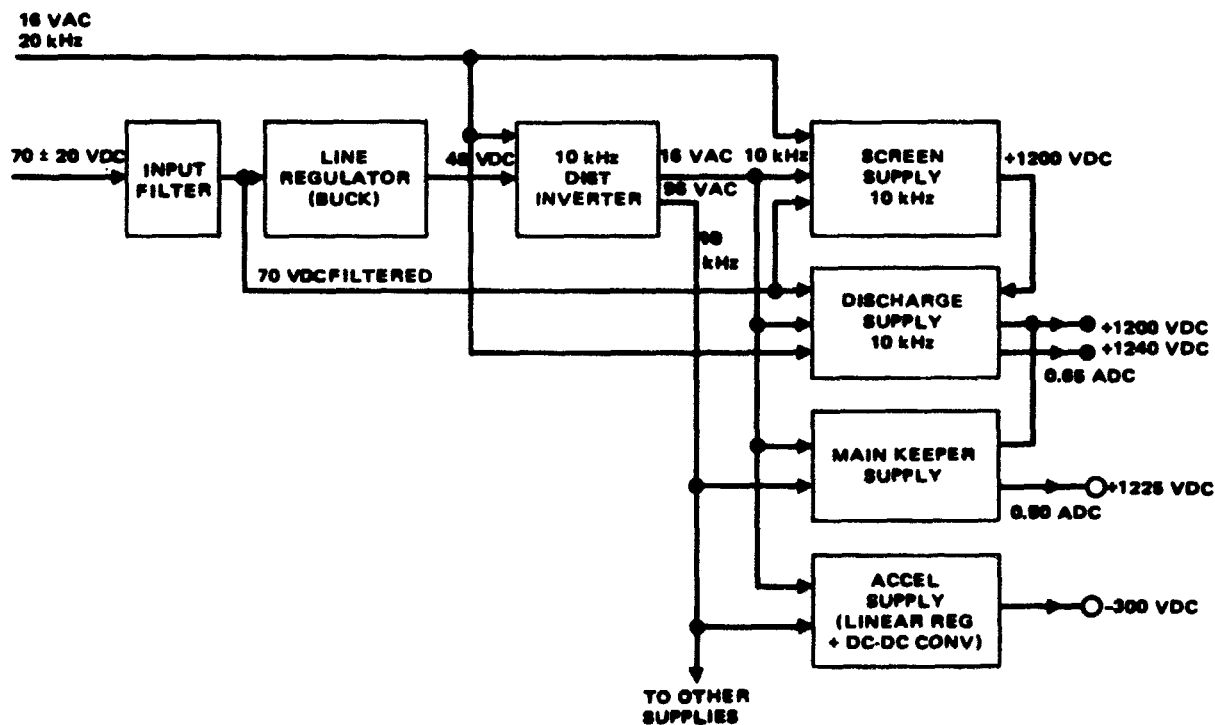


Figure 5-1. Partial block diagram of existing 8 cm ion engine PPU.

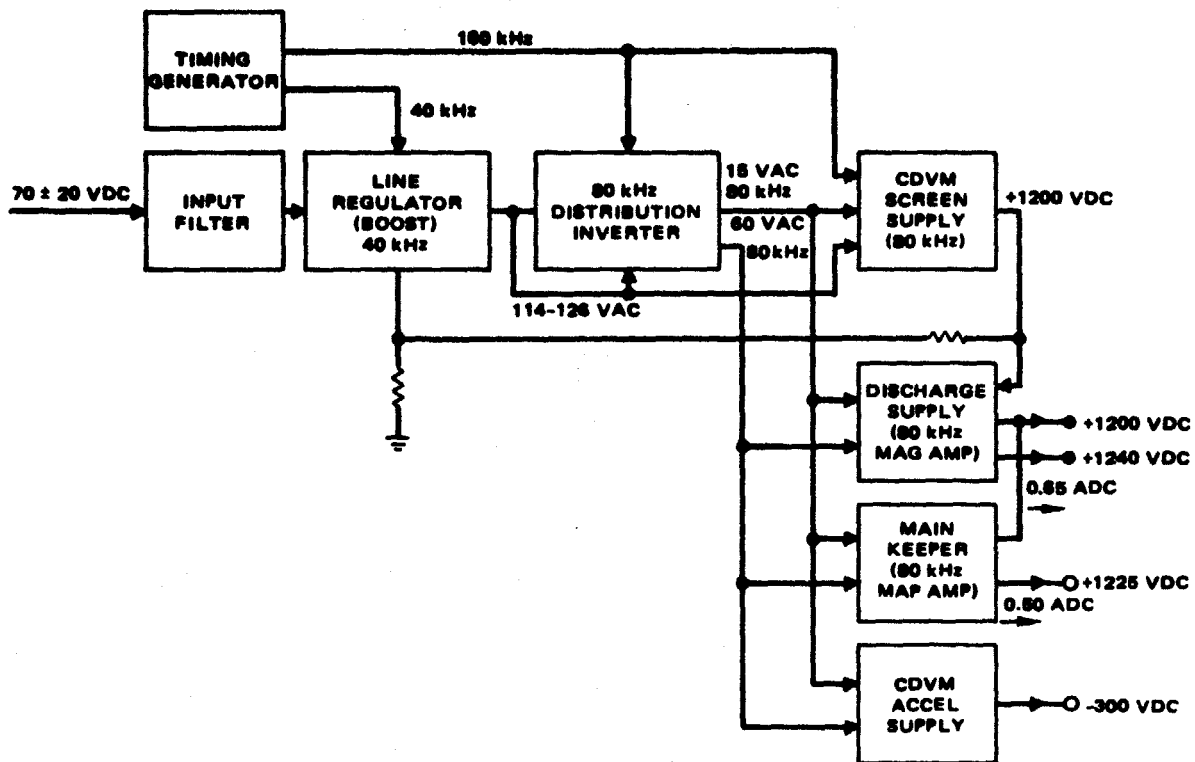


Figure 5-2. Partial block diagram of CDVM 8 cm ion engine PPU.

The high frequency CDVM based PPU design employed an input filter as before but followed by a boost converter preregulator operating at 40 kHz. Its output would be controllable over a narrow range, such as 114 to 126 Vdc. Voltage feedback from the 1200 Vdc CDVM output would control the regulator output so that the 1200 Vdc output would be regulated within the required 1 percent. The boost line regulator output would also drive a distribution inverter operating at 80 kHz. The distribution inverter would supply 15 V 80 kHz ac voltage to the CDVM screen supply, CDVM accel. supply, discharge and main keeper supplies, and 60 V, 80 kHz to the last three. A timing generator provides 160 kHz to the distribution inverter and CDVM screen supply, and 40 kHz to the boost line regulator.

Figure 5-3 is a schematic of a mag amp supply which was built to demonstrate feasibility of an 80 kHz circuit, and then was tested for regulation and efficiency. Output current regulation for the load and line

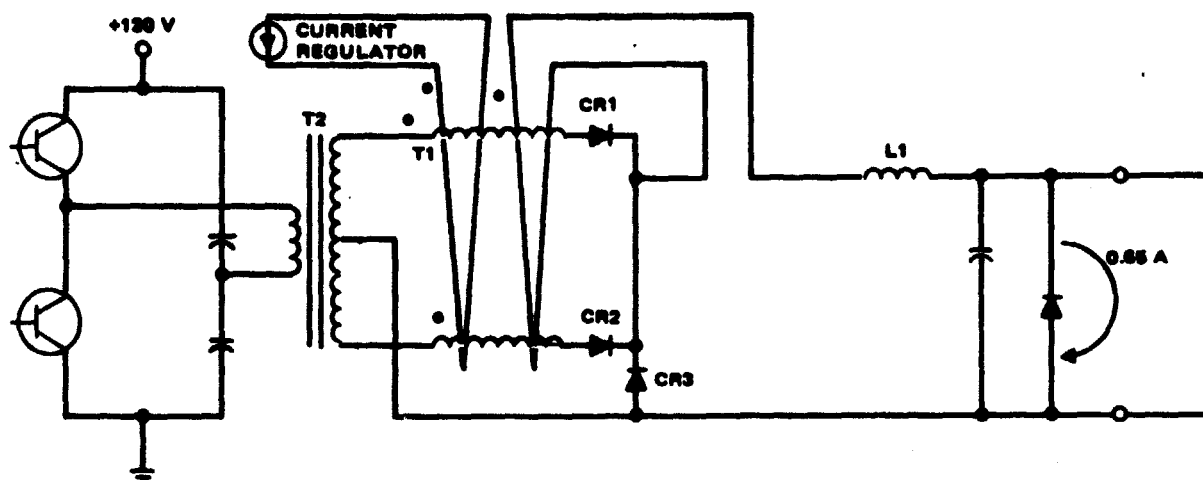


Figure 5-3. Magnetic amplifier current regulator.

conditions described in the specification for the discharge supply was within ± 1 percent at room temperature. The measured efficiency including the transistor chopper was 85 percent.

5.2 WEIGHT COMPARISON

Weight of the mag amp circuit, not including the transistor chopper (transistor chopper is included in the distribution inverter) is 80 grams total as shown in Table 5-2. This design was then used as a basis of comparison with the existing PPU in Table 5-3, which shows a component weight comparison for the four main output supplies, the distribution inverter, and line regulator. The high frequency design reduces the component weight by 557 grams or 42 percent. If comparable weight savings occurred as a result of extending the high frequency technology to the remaining supplies, one might expect a 42 percent maximum weight savings.

The weight of the packaged 8 cm design is approximately 6 kg (13 lbs). Based on previous experience at Hughes, the 557 grams of component weight savings for the four supplies listed in Table 5-3, in proportion would extrapolate to a packaged weight savings of 1100 to 1400 grams (2.4 to 3.1 lbs) for the total high frequency PPU. If the remainder of the supplies had no weight

TABLE 5-2. WEIGHT SUMMARY MAG AMP SUPPLY

	WT (grams)
Power Stage	
L1 (18 MM Pot Core)	14
T1 (2, 52056 - 1/2 D Cores)	28
T2 (18 MM Pot Core)	15
CR1 - CR3 (3FF50)	3
Control Circuit	
Filter Inductor	3
Op Amp	2
Resistors	8
Transistor	2
Capacitors	5
Total Weight	80 grams

TABLE 5-3. WEIGHT COMPARISON

	8 CM Ion Engine	CDVM Based Design
Screen Supply	378 grams	190 grams*
Main Keeper	151 grams	70 grams
Discharge Supply	329 grams	80 grams
Accel Supply	95 grams	46 grams
Distribution INV	140 grams	130 grams
Line Regulator	230 grams	250 grams
Total	1323 grams	766 grams
Weight Savings of CDVM Based PPU = 557 grams		
*Based on CDVM weight, less regulation circuitry.		

savings due to the high frequency design, then the overall savings would be 18 to 24 percent, instead of 42 percent.

5.3 EFFICIENCY COMPARISON

Overall efficiency of the 8 cm ion engine PPU was calculated at nominal line voltage of 70 V from the block diagram, Figure 5-4. Starting with the nominal wattage for each of the four outputs, and using efficiency estimates for the various blocks, the input wattage is 135.6 watts, for a 120.25 watts output.⁶ The ratio of these values gives an overall efficiency of 89 percent.

Following the same procedure for the CDVM PPU, shown in a block diagram, Figure 5-5, the input power calculates to be 139.4 watts for an overall efficiency of 86 percent. Efficiencies for the various blocks had to be estimated because data does not exist for the high frequency equivalents of Figure 5-4. If such estimates are accurate, then the high frequency CDVM would be 3 percent less efficient; however, before any final decision based on overall efficiencies is made measurements should be taken on the individual circuits in Figures 5-4 and 5-5.

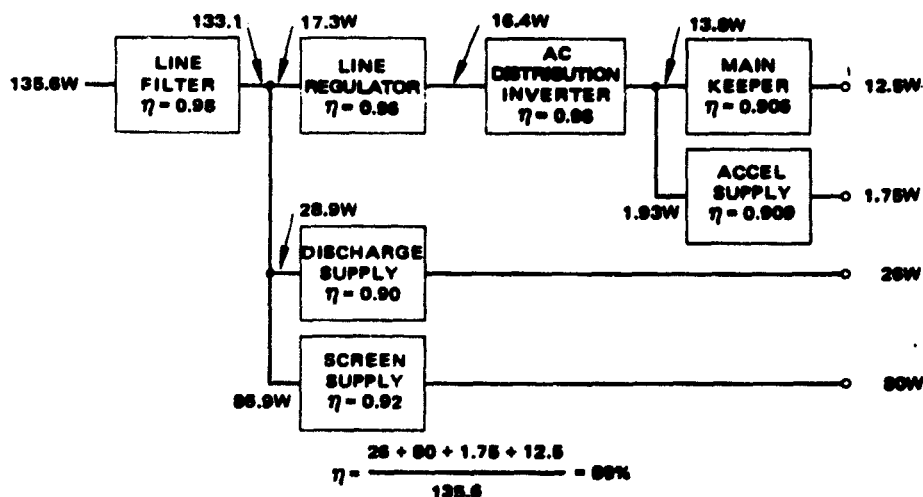


Figure 5-4. Efficiency block diagram of existing 8 cm ion engine PPU.

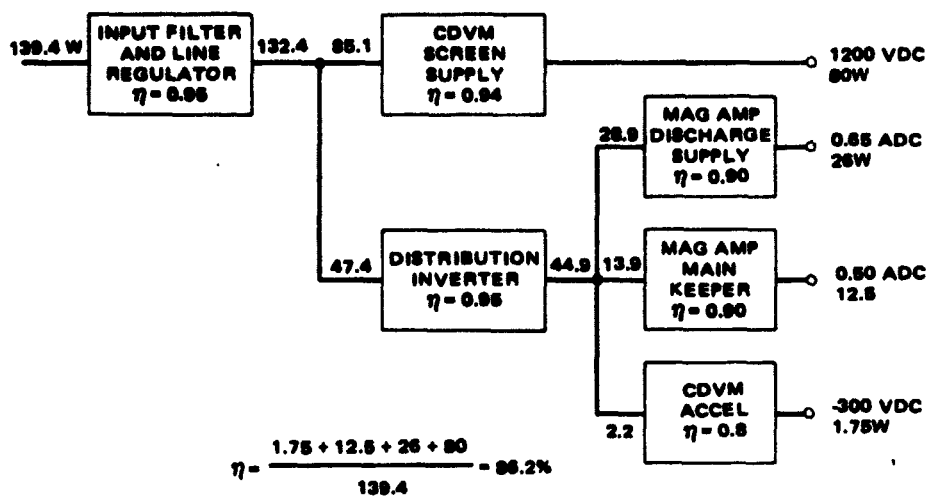


Figure 5-5. Efficiency block diagram of CDVM PPU.

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6.0 CONCLUSIONS AND RECOMMENDATIONS

- Work performed on this contract has advanced the state-of-the-art in capacitor-diode voltage multiplier power conversion equipment operating at higher frequencies than previously employed. In addition, the feasibility of obtaining multiple outputs from a CDVM, which characteristically is single output, was adequately demonstrated by tests of a four output bread-board operating at 80 KHz with a 120 W total power level.
- The maturity and flexibility of the technology was adequately demonstrated by employing a pair of two phase CDVMs, driven by the same two phase transistor chopper, and a pair of constant current supplies referenced to the high voltage rather than ground.
- Adequacy of the protective circuit design was demonstrated by short circuit tests of each output and interconnection of outputs.
- Comparison of the technology with an existing power processor design demonstrated that a considerable weight savings could be achieved at the possible expense of a minor reduction in efficiency.
- Design and packaging of a multiple output CDVM as a replacement of an existing system is recommended as a comparison. A possible candidate would be a complete high frequency PPU for the 8 cm ion engine, to determine actual advantages and disadvantages of this design.

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7.0 ACKNOWLEDGMENTS

Mr. Robert M. Martinelli of the Space and Communications Group was responsible for the circuit design, assisted in the Laboratory by Larry J. Murdy. Mr. William E. Michel provided valuable consultation on circuit design. Mr. Earle R. Bunker assisted in the preparation of the final report.

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APPENDIX A

BUCK REGULATOR EFFICIENCY CALCULATIONS

Calculation of the buck regulator efficiencies for both current supplies is done on a component by component basis, with the equations given below. Results are tabulated in Table 3-1.

Q_1 Switching:

$$P_{SW} = (t_r + t_f) f_{sw} \frac{V_{in} I_{sw}}{2}$$

Bridge Rectifier Forward Drop:

$$P_{(CR1 - 4)} = \frac{P_o}{m V_{in}} V_{FWD}$$

Q_1 Forward Drop:

$$P_{FWD} = V_{CE(ON)} I_{SW} \times \frac{t_{on}}{T}$$

Rectifier Forward Drop:

$$P_{(CR5)} = V_{FWD} I_L \frac{t_{off}}{T}$$

APPENDIX B
STATEMENT OF WORK

A description of the five tasks is given, followed by a tabulation of the Technical Requirements and Specifications for both Type I CDVM Biased Power Supply and Type II CDVM Biased Power Supply (Multiple Units).

The Contractor shall perform the work set forth below.

TASK I - TYPE I AND II CDVM BIASED POWER SUPPLY DESIGN

The Contractor shall design a low voltage high current-regulated power supply biased at high voltage by a capacitor diode voltage multiplier as shown in Figure 2-1. The CDVM design developed under other NASA contracts shall be evaluated and modified to meet the specifications given in this appendix under Technical Requirements and Specifications, Type I CDVM Biased Power Supply. The Type I CDVM biased power supply shall be a regulated buck boost circuit with pulse width modulation.

The Contractor also shall design multiple biased power supplies, three (3) operating simultaneously from an input of a capacitor diode voltage multiplier as shown in Figure 2-2. The performance specifications of the basic CDVM power supply and the three (3) biased power supplies are given in this appendix under Technical Requirements and Specifications, Type II CDVM Biased Power Supply (multiple units). The Contractor shall present his detailed design for approval to the NASA Project Manager before proceeding with Task II.

TASK II - FABRICATION OF TYPE II CDVM BIASED POWER SUPPLY

The Contractor shall fabricate one breadboard including multiple biased power supplies according to the design approved under Task II. These breadboards shall include the basic CDVM, the three biased power supplies, and all logic and control circuitry to operate the units.

TASK III - EVALUATION OF TYPE II CDVM BIASED POWER SUPPLY

The Contractor shall evaluate the multiple biased supplies fabricated under Task II. This evaluation shall include the following:

- Overall efficiency of the Type II CDVM biased multiple power supplies.
- Weight of the CDVM components.
- Weights of the individual buck boost circuit components.
- Voltage output of each of the biased power supplies as a function of the circuit power output.
- Biased supply output voltages, for all three supplies, as a function of CDVM load at 20 percent to 100 percent CDVM power output.

TASK IV - POWER PROCESSOR ASSESSMENT

The Contractor shall perform a study to estimate the component weight, and efficiency of a power processor system to meet the requirements as detailed in Table 5-1, 8 cm Ion Thruster Power Processor. The power processor shall incorporate the CDVM and biased supply technology developed under other NASA contracts.

TASK V - REPORTING REQUIREMENTS

1. Technical, financial, and schedule reporting shall be in accordance with the attached Reports of Work clause, which is hereby made a part of this contract.
2. The Contractor shall not report data in columns 7b, 9a, and 9b of NASA Form 533P.
3. The Monthly Contractor Financial Management Performance Analysis Report (NASA Form 533P), the Monthly Contractor Financial Management Report (NASA Form 533M), and the Monthly Technical Progress Narrative reports shall be due in

the offices of the addressees on or before the fifteenth calendar day of the month following the month being reported.

4. The number of copies to be submitted for each monthly report is as follows:
 - a. Fifteen copies of the Monthly Technical Progress Narrative.
 - b. Eight copies of the Contractor Financial Management Performance Analysis Report (NASA Form 533P), excluding columns 7 through 10.
5. The reporting categories to be reported in the Contractor's monthly reports are as follows:

NASA Form 533P, Monthly Contractor Management Performance Report, block 11 only

NASA Form 533M, Monthly Contractor Financial Management Report:

TASK I	Hours and Dollars	Type I and Type II Design
TASK II	Hours and Dollars	Type II Fabrication
TASK III	Hours and Dollars	Type II Evaluation
TASK IV	Hours and Dollars	Power Processor Assessment
TASK V	Hours and Dollars	Reporting Requirements
Subtotal	Hours and Dollars	
Fixed Fee	Hours and Dollars	
Fixed Fee	Dollars	

Total Resources Hours and Dollars

6. Within twenty working days after completion of the technical effort, the Contractor shall orally present a summary of the effort at the NASA Lewis Research Center.

TECHNICAL REQUIREMENTS AND SPECIFICATIONS

Type I - CDVM Biased Power Supply

VOLTAGE MULTIPLIER

Input voltage	120 $\pm$ 10 Vdc
Output voltage	1200 vdc
Output power	80 watts
Voltage regulation	1 percent
Output ripple	1 percent
Operating frequency	>50 kHz

BIASED SUPPLY

Output voltage	38 to 42 Vdc
Maximum output current	0.65 amp
Maximum output power	25 watts

Output current regulation	3 percent
Output current ripple	1 percent
Operating frequency	>50 kHz

The biased supply output current shall be controlled to within 20 mA of any selected current within the output current range of 100 to 650 mA.

Biased supply minimum efficiency	80 percent
Biased supply maximum weight	80 gms
Minimum overall efficiency (both supplies)	88 percent
Total power output (both supplies)	105 watts

Both supplies shall be current limited and self-protected.

Type II - CDVM Biased Power Supply (Multiple Units)

VOLTAGE MULTIPLIER

Input voltage	120 $\pm$ 10 Vdc
Output voltage	1200 $\pm$ dc
Output power	80 watts
Voltage regulation	1 percent
Output ripple	1 percent
Operating frequency	>50 kHz

BIASED SUPPLY NO. 1

Output voltage	38 to 42 Vdc
Maximum output current	0.65 amp
Maximum output power	25 watts
Output current regulation	3 percent
Output current ripple	1 percent
Operating frequency	>50 kHz
Minimum efficiency	80 percent
Maximum weight	80 gms

The output current of biased supply No. 1 shall be controlled to within 20 mA of any selected current within the output current range of 100 to 650 mA.

BIASED SUPPLY NO. 2

Output voltage	10 to 25 Vdc
Maximum output current	0.5 amp
Maximum output power	12.5 watts
Output current regulation	3 percent
Output current ripple	1 percent

Minimum efficiency	80 percent
Maximum weight	80 gms

The output current of biased supply No. 2 shall be controlled to within 15 mA of any selected current within the output current range 100 to 500 mA.

BIASED SUPPLY NO. 3

Output voltage	350 $\pm$ 10 Vdc
Maximum output current	0.005 amp
Maximum output power	1.7 watts
Output voltage regulation	3 percent
Output voltage ripple	1 percent
Operating frequency	>50 kHz

This supply shall be a separate three-stage voltage multiplier driven by the same chopper driving the main capacitor diode voltage multiplier specified above.

Type II CDVM power supply minimum efficiency shall be 90 percent or better. All supplies shall be current limited and self-protected.